Mapping of Multiple Data Flow Graphs of DSP Applications onto ASIC/Reconfigurable Architectures

Abstract: This paper presents a novel technique for the mapping of set of DSP applications onto architectures targeting an ASIC/Reconfigurable implementation embedded on the same chip. Synthesis for such a hybrid implementation is carried out by developing a technique to partition the RTL structures corresponding to a set of DSP applications into a fixed base design part suitable for ASIC implementation and a non-base design that varies with the applications and suitable for FPGA implementation. Experimental results reveal that the proposed scheme is efficient in exposing the hidden functional commonality in a set of RTL structures respecting some well-known benchmark problems. We show through a set of test cases that our approach offers significant area saving relative to the state-of-the-art.

Key words: DSP Data flow graphs, RTL structure, Graph merging, ASIC/reconfigurable platform