Efficient Techniques for Low Power Leakage Current Based on Header/Footer Techniques in Nano-scale Circuits

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ABSTRACT

In this paper we extensively analyze and evaluate the leakage current power dissipation based on the most popular Header/Footer approaches. Five different Nano-Scale SPICE parameters are used to evaluate each approach in this paper. An efficient approach based on Header/Footer technique to reduce the leakage current and increase the speed operation is proposed. Based on the new approach, it indicates that the SPICE parameters themselves decide rather than designer which approach it should employ (Header, Footer or Header & Footer), in order to achieve best low power reduction and high speed operation, comparison results between the proposed approach with other approaches are measured and analyzed.

Keywords— Footer Approach, Header Approach, Leakage Current, Nanotechnology.

1. INTRODUCTION

Switching to CMOS technology with a smaller scale dimensions offers higher performance and more compact chip size [1]. Unfortunately; leakage current is increasing as CMOS dimensions getting smaller causing higher static power dissipation [2]. Thus leakage power dissipation has become an important aspect in the two modes of operation which are active and standby. Based on the fact that scaling the dimension from one side, and reducing both of threshold voltage and oxide thickness from other side, could achieve high performance and high density. The revolution of Nano-technology which attracts a great attention these days [1][2] is faced by a major obstacle of the leakage current. This is because the transistor dimension scales down, the channel length is decreasing, which results in a higher leakage current (i.e. higher static power) [1-3]. Moreover, the threshed voltage keeps decreasing in recent technologies which lead to an increase in subthreshold leakage current, this happens due to the disability of the transistor to turn off completely in order to suppress the leakage current. The main two leakage currents appeared in nano-technology are the Gate Leakage which is dissipated when the transistor is in *on* or *off* states and Subthreshold Leakage which is dissipated only when the transistor is in *off* State. Since gate thickness is scaling faster than threshold voltage, it is expected that the gate leakage will grow faster than subthreshold leakage [1]. According to *ITRS* predictions [2], the static power will dominate below 65nm technologies.

Several approaches and techniques have been proposed to limit the effect of leakage current in nano-scale technologies [4-6]. One of these approaches is the Header/Footer, it has a good performance in reducing leakage current without adding considerable delay, thus in this paper we will focus on various approaches of this technique, and finally we present our own designs, that have more reduction power and lower delay time comparing with the previous designs.

The reset of this paper is organized as follows. Section 2 presents various leakage current reduction techniques, based on different Header/Footer techniques. Subsequently, section 3 demonstrates the experimental results, and comparison results between different approaches. Finally, the paper is concluded in Section 4. All of approaches are simulated based on nano-scale circuits.

2. LEAKAGE CURRENT REDUCTION TECHNIQUES

Various approaches and techniques are proposed and submitted in literature during the last decade to decrease the leakage current in transistor level [4-6], the leakage current appears in Nano-Scale SPICE parameters according to the following proportion,

$$I_{leakage} \propto W/L\,(1\text{-}e^{-q\,VTn\,/\,K\,T}) \quad (1)$$

Where W is the width of transistor, L is the length of transistor, q is the charge unit, V_{Tn} is the threshold voltage, K is constant, T is the temperature. In the following the main techniques of Header and Footer Techniques are discussed and analyzed.

2.1. Stack approach

The Stack approach [4] is based on minimizing ratio of the width and length by breaking each transistor into two halves. Each transistor in the pull-up or pull-down network is broken into to half size. It is evident to note that using this approach leads to double the total number of transistors in the circuit. Table I shows the effect of *W/L* for different predictive nanotechnologies.

Table I: W/L effect on leakage for different nanotechnologies.

W/L	22n	45n	65n
6	6.44E-05	1.13E-06	1.59E-08
4	2.76E-08	6.46E-10	1.05E-08
2	1.45E-11	4.95E-12	5.03E-09
1	2.60E-11	4.30E-12	8.65E-10

2.2 Sleep approaches

Due to the reasons mentioned previously, stack approach is not an efficient approach to reduce leakage current in nano-scale circuits. Further techniques have been proposed to avoid stack drawbacks. Most of these techniques are categorized under sleep transistor(s)

approach. It is very clear from equation (1) that the leakage is inversely proportional to the threshold voltage value V_T; thus one simple solution for leakage problem is to use transistors with high threshold voltage. Unfortunately, increasing the threshold voltage will increase delay time of transistor [5] which disagrees with the trend for next generation of SPICE parameters. So switching to high threshold voltage transistor is not feasible. In spite of this fact, the idea of employing a single high threshold transistor is presented in several papers [4][6][7]. This high threshold transistor is called sleep transistor because it limits leakage current when the circuit is operating in standby or sleep state.

The additional sleep transistor(s) is/are placed between the pull-up and/or the pull-down network to avert major part of leakage current. PMOS sleep transistor is placed between the V_{CC} and the pull-up network while the NMOS sleep transistor is placed between the ground and the pull-down network. The sleep transistor (either PMOS or NMOS) is turned *ON* when operating in active mode and turned *OFF* when operating in standby (sleep) mode. It acts like as a resistance that disconnects the circuit from the power supply when operates in sleep mode.

2.3 Super leakage current cut-off approaches

In addition to the Header/Footer techniques mentioned before, there are other techniques which are able to achieve higher leakage current reduction. These techniques maybe be used for ultra low power (rather than low power) applications, in this section we mention some of these approaches and their advantages and disadvantages.

A. Boosted gate approach

The boosted gate approach employs high threshold thick oxide sleep transistors [9]. Thick sleep transistors are more efficient in reducing leakage current, because gate leakage increases as oxide thickness decreases [3] [9]. To maintain high operation speed, the rest of the circuit is composed of low threshold thin oxide transistors.

B. Supply switching with ground collapse (SSGC) approach

This technique achieves high leakage reduction in nano-scale circuits [10]. As Footer implementation, a high threshold PMOS is placed between the supply voltage and the pull-up network. Additional low threshold NMOS or low threshold PMOS is placed in parallel with sleep PMOS. The drain of the high threshold PMOS is connected to V_{CC} while the low threshold PMOS/NMOS is connected to a fixed predefined voltage V_{sb}. The low threshold transistor is turned *off* during the active mode, while the high threshold transistor is turned *off* during standby mode to reduce leakage current.

C. Proposed Header/Footer approach

In addition to the sleep transistor techniques mentioned above, we proposed efficient Header/Footer techniques in reducing the leakage current and increasing in the speed operation. The above approaches use determinately PMOS transistors as Header and other NMOS as Footer regardless the value of the threshold voltage transistors of PMOS and NMOS. This difference between threshold of PMOS and NMOS transistors could achieve more power reduction, the influence of threshold voltage on reducing power dissipation is analyzed in details in [10]. In this case, when the threshold voltage of PMOS transistor (V_{TP}) is greater than the threshold voltage of NMOS transistor (V_{TN}), then it is preferable to use two PMOS transistors as Header and Footer transistors, while if the V_{TN} of NMOS transistor is greater than the V_{TP}, then it is preferable to use two NMOS transistors as Header and Footer transistors. Simulation results verified this concept and achieved better results than the conventional design, the proposed approach is shown in Figure 1.

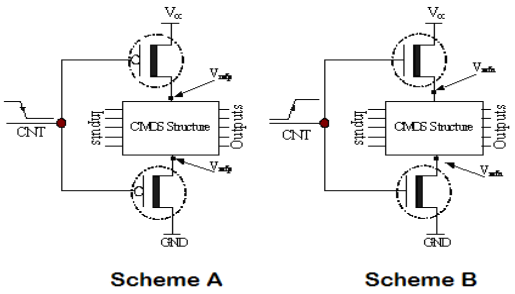

Figure1: Proposed Header/Footer schemes

Even this technique suffer from the low swing voltage technique in Case B, but it still preferable in case of low leakage current.

3. SIMULATION RESULTS

As it is mentioned before, there is no clear reference compares between the Header/Footer techniques and evaluates their performance. In this paper, it performs extensive comparisons and simulations for the known sleep transistor approaches for different circuits using different SPICE parameters technologies. In the simulations they used the predictive CMOS technology models for 16nm, 22nm, 45nm, 65nm and 90nm technologies, these set of parameters are found on [1], HSPICE is used as the simulation tool.

3.1. Leakage current analysis

Figure 2 compares the leakage current for a chain of 3 inverters for the conventional approach and stack approach. It is obvious that stack approach result in leakage current reduction. This is a consequence of breaking each transistor into to half size transistors. It is evident to note the increase in leakage current as the supply voltage increases. Combing the two sleep transistors PMOS (Header) and NMOS (Footer) has a superior result in minimizing leakage current.

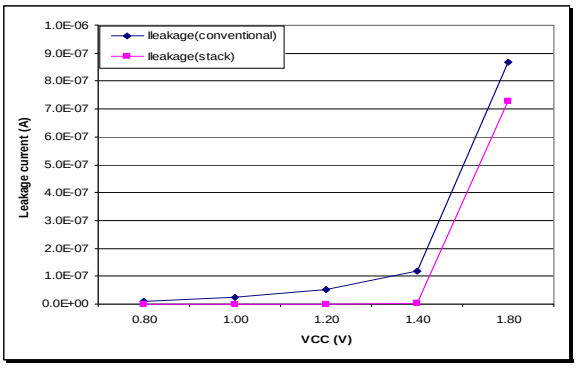

Figure2: Leakage current for a chain of Three inverters at different V_{CC} values (22nm technology).

This is because the high threshold sleep transistors cooperate together to reduce the standby current to the minimal value. Table II shows more clear the analysis shown in Figure 2.

Table II: Header/Footer Leakage current for a chain of 3 inverters voltages (65nnm parameters).

VCC	Without H/F	Header	Footer	Header & Footer
0.8	5.29E-10	2.51E-10	1.84E-10	1.65E-11
1.0	1.76E-09	1.03E-09	5.93E-10	6.48E-11
1.2	5.45E-09	3.95E-09	1.80E-09	4.65E-10
1.4	1.60E-08	1.59E-08	5.30E-09	5.09E-09
1.8	2.46E-07	2.43E-07	1.24E-07	1.21E-07

Figure 3 shows the results for attaching Header transistor, Footer transistor and Header & Footer transistors to the 1-bit full adder base case, for all input combinations. Clearly, a considerable amount of leakage reduction is achieved when the sleep transistors are applied however; the best reduction ratio is achieved when both Header and Footer sleep transistors are used together.

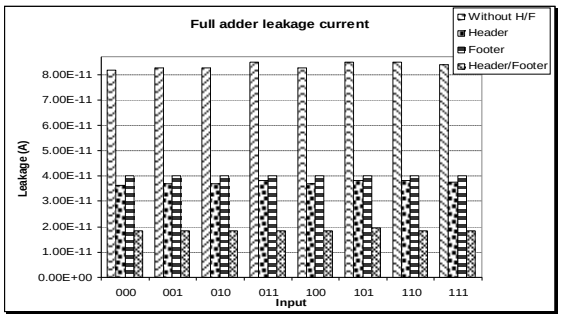

Figure3: The performance of Header, Footer, Header&Footer for 1-bit full adder (22nm technology).

Table III below illustrates comparison results between the mentioned approaches and the conventional one (without any modification). It shows that the Header/Footer technique has the superior result in reducing leakage current regardless the underlying circuit attached to.

Table III: leakage current for the sleep transistor approaches and base case for 65nm technology parameters.

Circuit	without	Stack	H/F	Zigzag	Sleepy
1_Inv	2.98E-9	3.5E-10	1.82E-12	8.68E-11	4.096E-12
3_Inv	9.90E-09	1.0E-09	5.48E-12	4.79E-10	1.22E-11
AND	2.47E-08	5.3E-09	1.03E-11	1.38E-09	2.17E-11
OR	2.77E-08	7.2E-09	1.27E-11	1.57E-09	3.24E-11
FA	7.10E-07	7.2E-08	3.66E-10	4.31E-08	7.56E-10

A. The influence of threshold voltage on Header /Footer techniques

As the main purpose of this paper is to give special focus and extensive simulations for Header/Footer techniques in order to reveal some facts that may help the designers employing the most efficient scheme. Table IV shows the leakage current reduction ratios for Header and Footer techniques using 65nm and 32nm SPICE parameters.

Table IV: leakage current reduction ratio for Header and Footer schemes.

	65nm Technology		32nm technology	
VCC	**Header**	**Footer**	**Header**	**Footer**
0.8	52.60%	65.20%	83.90%	56.80%
1.0	41.50%	66.30%	79%	53.90%
1.2	27.50%	76%	76.20%	52.40%
1.4	0.63%	67%	75%	50.80%
1.8	1.22%	49.60%	84.30%	24.50%

For the 65nm technology, the PMOS threshold voltage is smaller than NMOS threshold voltage, but for the 32nm technology PMOS threshold voltage is higher than NMOS threshold voltage. It shows clearly that Footer approach has much better ability to reduce leakage current in 65nm technology, whereas for 32nm technology the Header approach has the superior capability in reducing leakage current. Accordingly we can state that Header approach performs better than Footer approach if PMOS threshold is greater than NMOS threshold, while Footer achieves better performance if the NMOS threshold is greater than PMOS threshold. This result should be kept in mind when the designer is going to choose between Header or Footer techniques.

B. Leakage current analysis for the proposed schemes

In the previous section, we proved that some SPICE parameters like threshold voltage affect the performance of Header/Footer approaches. When the Header offers higher capability in reducing leakage current, we suggest using PMOS sleep transistor for both the Header and the Footer, and using NMOS for both Header and Footer sleep transistors when the Footer offers higher leakage current reduction. The validity of this proposed idea is shown in Figure 4, where the proposed schemes (*a*) and (*b*) are better than the conventional Header/Footer approaches.

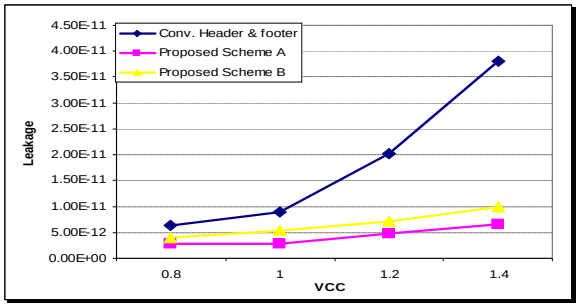

Figure 4: Comparison between proposed Header/Footer and the conventional Header/Footer schemes.

3.2. Static power analysis

Static power is directly proportional to the leakage current, thus it is desirable to reduce leakage current thereby reducing static power dissipation. The static power dissipation for the different Header/Footer schemes is shown in Table V.

Table V: Header/Footer static power dissipation (22nm)

VCC	Without H/F	Header	Footer	Header & Footer
0.8	1.31E-11	7.84E-12	3.62E-12	1.40E-12
1	6.83E-11	4.51E-11	5.21E-12	1.67E-12
1.2	2.25E-10	1.57E-10	7.96E-12	2.22E-12
1.4	1.58E-09	9.27E-10	2.57E-11	2.80E-12
1.8	5.44E-07	2.76E-07	1.79E-08	4.46E-12

Table VI shows the performance of different types of applications based on Different Header/Footer techniques and their performances.

Table VI: Static power dissipation for the sleep transistor approaches and base case for 65nm technology parameters.

Circuit	Without H/F	Stack	H/F	Zigzag	Sleepy keeper
1 inv	2.38E-9	2.8E-10	1.46E-12	6.94E-11	3.28E-12
3 inv's	7.92E-09	8.56E-10	4.38E-12	3.83E-10	9.76E-12
AND_2	1.97E-08	4.25E-09	8.24E-12	1.1E-09	1.74E-11
OR_2	2.22E-08	5.74E-09	1.02E-11	1.26E-09	2.59E-11
FA_1bit	5.68E-07	5.78E-08	2.93E-10	3.45E-08	6.05E-10

Figure 5 shows the static power dissipation for the conventional Header/Footer and our proposed schemes in Figure 1. In terms of static power dissipation scheme A and scheme B of our proposed approach has lower static power dissipation than the conventional Header/Footer static power dissipation.

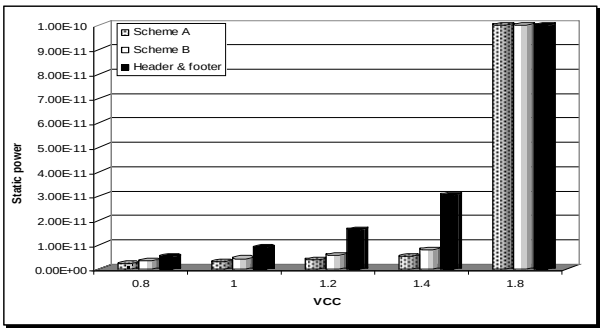

Figure 5: The static power dissipation for the conventional Header/Footer schemes and our proposed schemes.

3.3. Delay analysis

The Delay time is an important parameter that must be considered when designing circuits. The performance of the sleep transistor approaches is shown in Figure 6. It is evident to note that the sleepy stack approach has the highest delay. The sleep transistors have high threshold, and as transistor threshold increase the delay increases as well. Zigzag approach has a delay lower than Header/Footer scheme because it uses either Header or Footer sleep transistor for each circuit making up an alternating sequence of Header and Footer thus has lower delay because sleep transistors have high threshold.

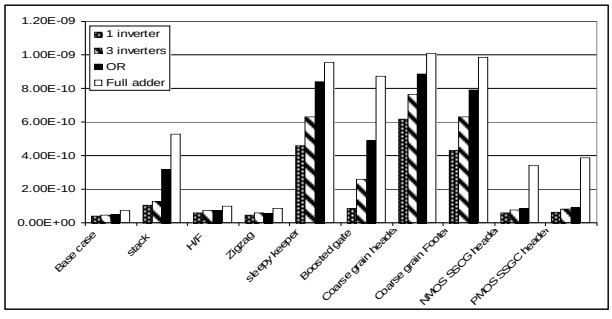

Figure 6: The delay for sleep transistor schemes for different circuits (45nm technology).

As shown in Figure 6, the coarse grain approaches have the highest delay. This is because it adds several high threshold transistors in parallel and the delay increases as the threshold increases. Boosted gate has high propagation delay because it employs high thickness transistors and the delay increases if the oxide thickness increases.

Figure 7 demonstrates the delay for conventional Header/Footer and the proposed schemes. Scheme B has the lowest propagation delay, this is because it employs two NMOS sleep transistor rather than using any sleep PMOS.

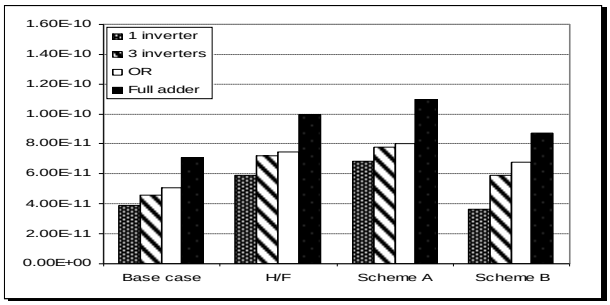

Figure 7: The delay for the conventional Header/Footer techniques and the proposed one.

3.4. conclusion

In this paper we examined the performance of different leakage reduction techniques based on Header/Footer technique in terms of leakage current and static power & propagation delay. The importance of this paper comes from the fact that no such paper studies extensively leakage reduction techniques. We proveded that the selection between Header/Footer techniques must not be done arbitrary; rather SPICE parameters control this selection. We stated that Header technique performs better than Footer when PMOS threshold has higher threshold voltage than NMOS; whereas Footer technique performs better when the NMOS threshold is higher. Finally, we proposed two Header/Footer techniques that employ this idea.

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