Abstract

This work uses switch-level Verilog to simulate entire benchmarks using transistor level schematics and post-layout capacitance extraction. By translating a schematic netlist into a transistor level Verilog netlist, thousands of benchmark cycles can be simulated in minutes or hours compared with only tens of cycles using a fast spice simulator. This difference in simulation speed enables simulating an entire benchmark instead of trying to guess what a good spice simulation window is. This flow has been used extensively for power estimation and optimization of custom-based cache designs integrated into Qualcomm's 45 nm low power DSPs.