

Abstract

Steganography is one of the most powerful techniques to conceal the existence of hidden secret data inside a cover object. Images are the most popular cover objects for steganography, and thus the importance of image steganography. Embedding secret information inside images requires intensive computations, and therefore, designing steganography in hardware speeds up steganography. This work presents a hardware design of Least Significant Bit (LSB) steganography technique in a cyclone II FPGA of the Altera family. The design utilizes the Nios embedded processor as well as specialized logic to perform the steganography steps. The design balances the tradeoffs such as imperceptibility, quality and capacity.