A Hybrid Scheme for Minimizing Leakage Current in CMOS-Based Architectures by Employing Multiple Supply Voltages and Power Gating Techniques

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***Abstract*— In recent years, power dissipation in Integrated Circuits (IC's) is becoming a crucial factor with technology shrinking down to deep submicron. Furthermore, with level of parallelism becoming a big issue [1, 2], the more processed data the more heat by integrated circuits is produced which in turn affects the system life, especially for handheld equipments (i.e., Mobile phones, Tablets, Laptops. etc). Such equipments needs to stay a life as maximum as possible on the same battery capacity. Hence, the choice is either to enlarge battery capacity which in turn lays on big costs or to decrease the power consumption which seems the ideal solution. For <100 nm architectures most of power is being consumed as a leakage power produced by leakage currents [3, 4]. In this paper, a new hybrid technique is proposed by employing both, multiple supply voltages and power gating approaches, aiming at minimizing the leakage current. The proposed hybrid model is shown to bring about good improvement in terms of power dissipation**

keywords—Power Gating, Leakage, Dissipation, CMOS, Integrated Circuits