Awni Hussein Itradat

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RESEARCH INTERESTS

General research areas are high-level synthesis and parallel architectures. Research interests include scheduling and resource allocation, reconfigurable computing, ASIC synthesis, graph theory, Network on chip, and computer architecture and organization.

ACADEMIC QUALIFICATIONS

- A Ph.D in Computer Engineering, Concordia University, Canada **(2004-2008).**
- Master of Applied Science in Electrical and Computer Engineering, Concordia University, Canada **(2002-2004**).
- Bachelor of Electrical Engineering (Computer Engineering), Jordan University of Science and Technology; Irbid, Jordan. **(1995-2000)**
- General Certificate of Education, Science Stream, Irbid, Jordan **(1995).**

WORK EXPERIENCE

- **2009-to-date**, Chair of the Department of Computer Engineering, Hashemite University, Jordan.
- **2009-to-date**, Assistant Professor, Department of Computer Engineering, Hashemite University, Jordan.
- **2002-2008**, Research assistant at Dept. of Electrical and Computer Engineering at Concordia University, Canada.
- **2004-2008,** VLSI Research Coordinator, Dept. of Electrical and Computer Engineering at Concordia University, Canada.
- **2000-2001,** IT Faculty Reperesentative to the Computer and Information Center, Jordan University of Science and Technology, Jordan.

- **Jan 2001 – Dec 2001,** Working as an Instructor at the Department of Computer Engineering – Jordan University of Science and Technology, teaching Micro-system Lab, Maintenance Lab, microprocessor and their applications, computer organization.

- **Sept 2000 – Dec 2000**, Working as Lab Engineer in Yarmouk University "Al-hejjawi Faculty" (**digital labs, programming**), Jordan**.**

TEACHING EXPERIENCE

- **2009-to-date,** Teaching different courses at the Department of Computer Engineering, Hashemite University, i.e., Assembly Language, Microprocessor Based Systems, Digital Logic, Computer Maintenance**.**

- **Sept. 2008 – Dec. 2008,** Teaching assistant for the Lab **COEN417 (Microprocessors and Interfacing)**, Concordia University, Canada.

- **Jan. 2008 – Sept. 2008,** Teaching assistant for the Lab **COEN312 (Digital design)**, Concordia University.

- **Sept. 2007-Dec 2007,** Teaching assistant for the Lab **COEN417 (Microprocesors and interfacing)**, Concordia University.

- **Jan. 2007-April 2007,** Teaching assistant for the Labs **COEN311 (Computer organization)** and **COEN312 (Digital design)**, Concordia University.

- **Dec. 2006,** Teaching of the undergraduate course **COEN417 (Microprocessors and their applications)** for short-period (Replacing the instructor), Concordia University.

- **Sept. 2006-Dec. 2006,** Teaching assistant for the Labs **COEN311 (Computer organization)** and **COEN417 (Microprocessors)**. Concordia University.

- **Sept. 2005-April 2006,** Teaching fellowship**, Circuit analysis ELEC273.**

- **Sept. 2004 – Dec. 2004,** Teaching assistant for **EMAT 213 (Differential equations) and EMAT 233 (Advance math.).** Concordia University

- **Jan. 2003-May 2003,** Working as Programmer on Duty **(POD)** at Dept. of Electrical and Computer Engineering at Concordia University.

- **Sept 2000 – Dec 2000**, Working as teacher assistant for digital and assembly labs, Yarmouk Unversity, Jordan**.**

- **Jan 2001 – Dec 2001,** Working as teacher assistant for digital, microprocessor, electronic, and circuits labs, Jordan University of Science and Technology.

HONORS AND AWARDS

- **May 2002 – May 2009,** Research Assistantship, Concordia University, Canada.
- **May 2008,** Student Travel Award to attend the International Symposium of Circuits and Systems, ISCAS 2008, School of Graduate Studies-Concordia University.
- **May 2007,** Selected as one of the top five papers in IEEE-ISCAS 07-The architecural synthesis track.
- **June 2008,** Selected to be Granted the registeration fees and travel expenses in IEEE-NEWCAS 08.
- **Sept. 2005 – Dec. 2005,** Teaching Fellowship, Concordia University.
- **Jan. 2006 – May. 2006,** Teaching Fellowship, Concordia University.
- **2005**, Concordia International Graduate Tuition Scholarship.
- **2004 – 2008,** Scholarship from the Hashemite University-Jordan to complete a Ph.D. degree at Concordia University.
- **2004,** Partial Scholarship for International Students, Concordia University.
- **2003,** Partial Scholarship for International Students, Concordia University.
- **2001,** Distinguished leadership employee in the Jordan University of Science and Technology.
- **1995 – 1997,** Scholarship for distinguished undergraduate students from Ministry of Higher Education and Scientific Research, Jordan.
- **1999 – 2000,** Scholarship for distinguished undergraduate students from Ministry of Higher Education and Scientific Research, Jordan.

PUBLICATIONS

1. A. Itradat, M.O. Ahmad, A. Shatnawi, **"High-level Architectural Synthesis of DSP Data Flow Graphs with Inter-Processor Communication Delays,"** Accepted for publication *IET Journal on Circuits, Devices*.

2. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Interconnect-Aware Register Binding with and without Node Regeneration for High-Level Synthesis,"** Accepted with Minor revision for possible publication In *IEEE Transaction on Computer Aided Design for Integrated Circuits and Systems.*

3. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Incorporating of Reconfigurable units in a Simultaneous Scheduling, Allocation, and Placement with Interprocessor Communication Delay,"** Submitted for possible publication in *IEEE Transaction on Computer Aided Design for Integrated Circuits and Systems.*

4. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Delay and sampling-rate aware architectural synthesis in presence of communication overhead,"** In *The 3rd International IEEE-NEWCAS 2008 Conference*, Quebec, Canada, 22-25 June 2008, Page(s): 323 – 326.

5. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Minimization of I/O delay in the architectural synthesis of DSP data flow graphs,"** in *the IEEE International Symposium on Circuits and Systems. ISCAS 2008*, Seattle, USA, May 18-21, 2008, pp. 205 - 208.

6. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Architectural synthesis of DSP applications with dynamically reconfigurable functional units,"** In *the IEEE International Symposium on Circuits and Systems. ISCAS 2007*, New Orleans, USA, 27-30 May 2007, Page(s):1037 - 1040.

7. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Dynamically reconfigurable adaptable multi-module based synthesis of DSP data flow graphs,"** In *IEEE Canadian Conference on Electrical and Computer Engineering 2007*, CCECE 2007, Vancouver, Canada, 22-26 April 2007, Page(s):1515 – 1518.

8. A. Itradat, M.O. Ahmad, A. Shatnawi, **"A processor allocation of DSP applications onto heterogeneous multiprocessor architectures,"** In *IEEE Canadian Conference on Electrical and Computer Engineering 2007*, CCECE 2007, Vancouver, Canada, 22-26 April 2007 Page(s):944 - 947.

9. A. Itradat, M.O. Ahmad, A. Shatnawi, "**A delay-optimal static scheduling of DSP applications mapped onto multiprocessor architectures,"** In *the IEEE International Symposium on Parallel Computing in Electrical Engineering 2006, PARELEC 2006.*, Bialystok, Poland, 13-17 Sept. 2006, Page(s):386 – 391.

10. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Incorporation of reservation stations into the scheduling of DSP graphs onto heterogeneous multiprocessors,"** In *IEEE 48th Midwest Symposium on Circuits and Systems, MWSCAS 2005*, 7-10 Aug. 2005, Cincinnati, USA, Vol. 1, Page(s):460 - 463.

11. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Scheduling of DSP algorithms onto heterogeneous multiprocessors with inter-processor communication,"** In *The 3rd International IEEE-NEWCAS 2005 Conference*, Quebec, Canada, 19-22 June 2005, Page(s):95 – 98.

12. A. Itradat, M.O. Ahmad, A. Shatnawi, **"Scheduling of DSP data flow graphs with processing times characterized by fuzzy sets,"** In *Canadian Conference on Electrical and Computer Engineering 2004* , IEEE CCECE 2004, Niagara Falls, Canada, 2-5 May 2004, Vol. 3, Page(s):1245 – 1248.

PROFESSIONAL SERVICES

- Member of different Faculty and Departmental committees at Hashemite University 2009.
- The decision of the Commission for different projects and studies in the Engineering Faculty and the Department of Computer Engineering, Hashemite University.
- Reviewer for several international journals and conferences. e.g. IEEE Transactions on Circuits and Systems(IEEE-TCAD) and IEEE Transaction on VLSI; IEEE Int. Symposium on Circuits and Systems (ISCAS); ACM Conf. on Compilers, Architecture, and Synthesis for Embedded Systems (CASES); ACM Transactions on Architecture and Code Optimization (TACO); IEEE Int. Conf. on Parallel Computing (IEEE-PARELEC).
- Member of the international advisory board for the International Congress on Pervasive Computing and Management (ICPCM), 2008.
- A Member in many of the establishing committees of IT faculty in JUST, 2000-2001.
- Participated in the organization of the 2nd International Arab Conference on Information Technology, 13-15 Nov. 2001, JUST.
- Chairing the Engineers section in the IT faculty of JUST, 2000 – 2001.
- Significantly contributed in the design of the Computer Engineering Labs of the IT faculty in Jordan University of Science and Technology (JUST) 2000-2001.
- Participated in several technical committees for tenders pertaining to the Computer and Information Center (ICT) infrastructure of JUST 2000-2001.
- Trainer in the computer literacy ICDL project, 2001.

COMPUTER SKILLS

- Platforms: Windows, Unix.
- Programming Languages: C/C++, Java
- Tools: Mentor-Graphics Tools (ModelSim., Leonardo synthesis tool) , Xilinx synthesis tool, Maple, Matlab, Microsoft Office.
- Hardware Design Languages: VHDL.
- Verilog, Matlab, Spice.

MAJOR PROJECTS AND FUNDS

- Preparing the proposal for quality assurance workshop on the Higher Eduation in Jordan, will be organized by the Hashmite University, Sponsored by Al-Hussien Fund for Excellence, 2009.
- Participate in establishing the IT incubator at the Department of Computer Engineering, Hashemite University (Funded Project), 2009.
- Participate in establishing a VLSI Lab. at Concordia University, Canada, Sponsored by NSERC-Canada 2006-2007.

TRAINING

- Java: 50 hour training at STS
- Rational Rose: 50 hour training
- Leading and Management training, Canada.
- Web Publishing and Online Teaching Tools (FrontPage, WebCT, Blackboard)

PROFESSIONAL AFFILIATIONS

- Member of ACM: Association for Computing Machinery.
- Member of IEEE: Institute of Electrical and Electronics Engineers
- Member of IEEE Computer Society.
- Member of IEEE Circuits and Systems Society.
- Member of Jordan Engineers Association.

PERSONAL INFORMATION

- **Date and Place of Birth:** Jan 6-1977, Jordan.
- **Marital Status:** Married with one son and three daughters

REFERENCES **(Available Upon Request)**