CHAPTER EIGHT

Schottky Transistor-Transistor logic (STTL)

Digital Electronics.

Introduction

Transistor-Transistor Logic (TTL) ⇒ **Schottky Transistor-Transistor Logic (STTL)**

STTL is obtained by replacing the BJT with Schottky-clamped BJT (SBJT)

The primary advantage of SBJTs is their improved transient times since SBJT does NOT operate in saturation

Schottky-Barrier Diodes (SBD)

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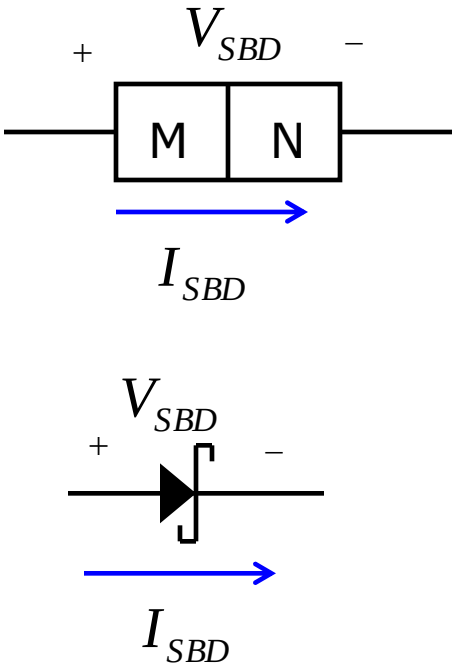
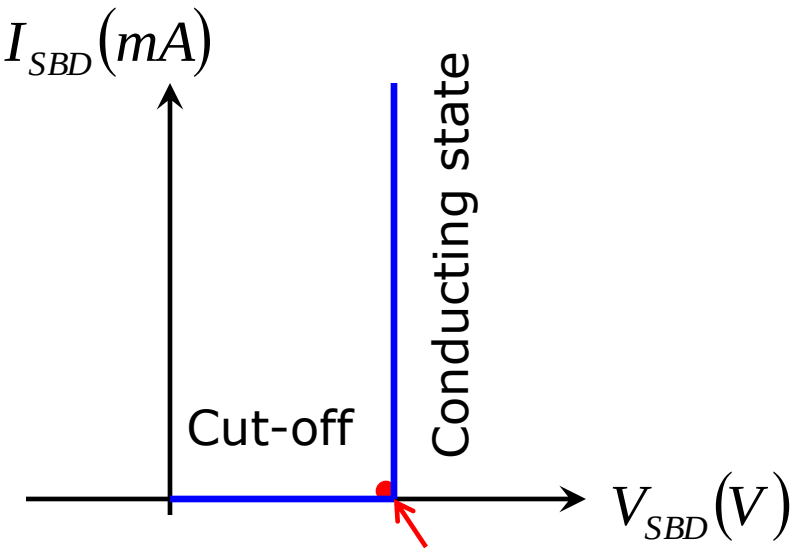
Schottky-barrier diode is made by adjoining **m**etal and **N**-type semiconductor (usually aluminum with N-type silicon)



Circuit symbol



Current voltage characteristics

Schottky-Clamped SBJT

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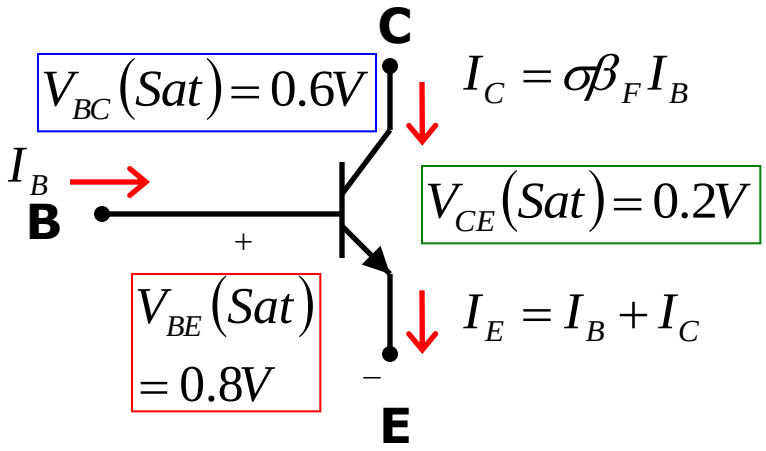


Saturation Mode

A serious problem that limits the switching speed of a BJT inverter as well the TTL gates is the time required to remove the enormous stored charge of the base of a saturated BJT.

Thus, the solution is to use BJTs that do not saturate.

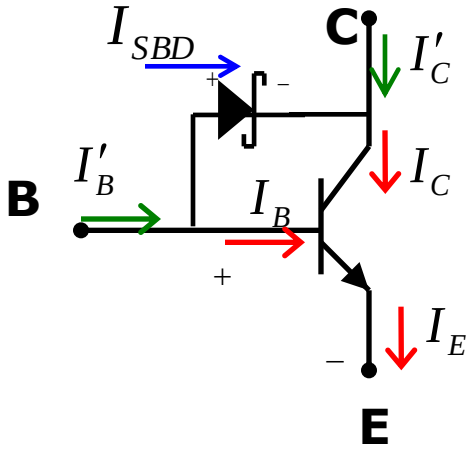
The saturation can be avoided by limiting the forward-biased base-collector voltage to values less than 0.6 V

The saturation mode is characterized by the forward biased B-C voltage

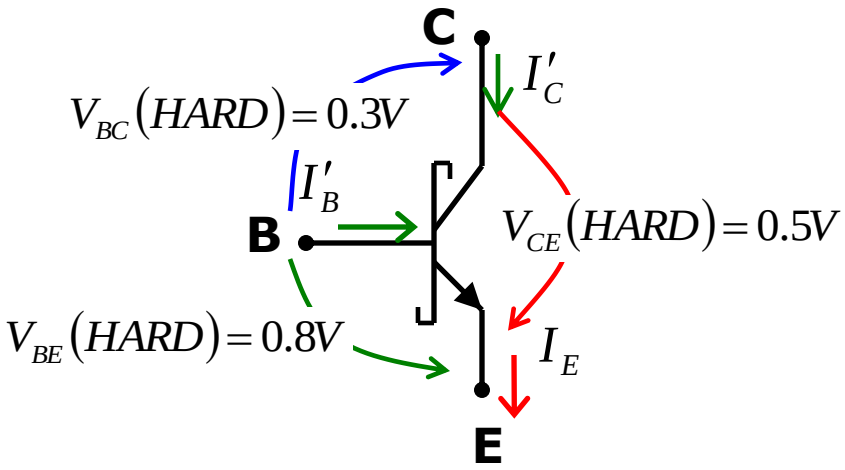
$$V_{BC}(sat)=V_{BE}(sat)-V_{CE}(sat)$$
$$=0.8-0.2=0.6V$$

This is accomplished by placing SBD across the base and collector terminals of a BJT.

Schottky-Clamped SBJT



Equivalent circuit



Circuit symbol

Schottky-Clamped SBJT

"Inverse-active" Schottky Mode:

Since V_{BC} is limited to $V_{SBD}(ON)=V_{BC}(HARD)=0.3V$
$V_{BC}(RA)=0.7V$

The SBJT can not operate in inverse active mode

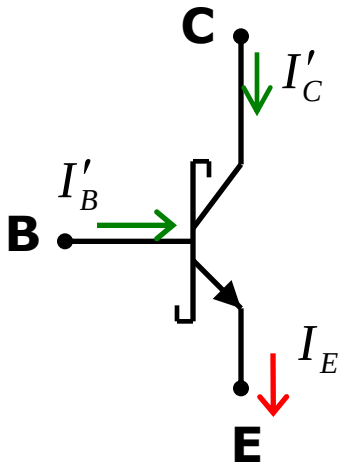
However, for

$$V_{BE} < V_{BE}(FA),\ V_{BC} = V_{BC}(RS) = 0.3V$$

$$I'_C = -I_{SBD}$$

$$I'_B = I_{SBD}$$

$$I_B = I_C = I_E = 0$$



Schottky-Clamped SBJT

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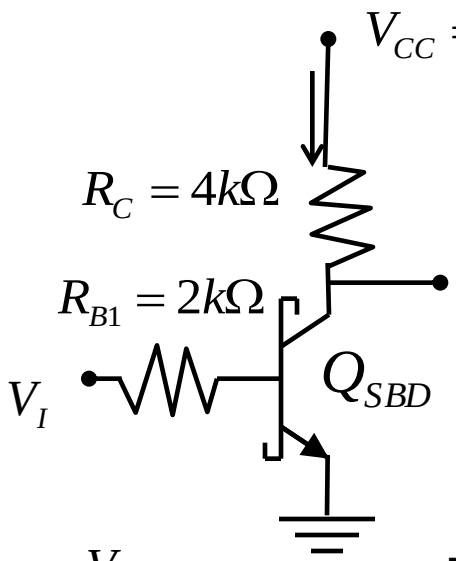
- Example

Determine the logic swing of SBJT shown, assuming



- Solution

V_{OH} When V_I is low, SBJT is cut-off

$I_{RC} = I_C = 0 \quad V_{OH} = V_{CC} = 5V$

V_{OL} → SBJT is "ON-HARD" mode,

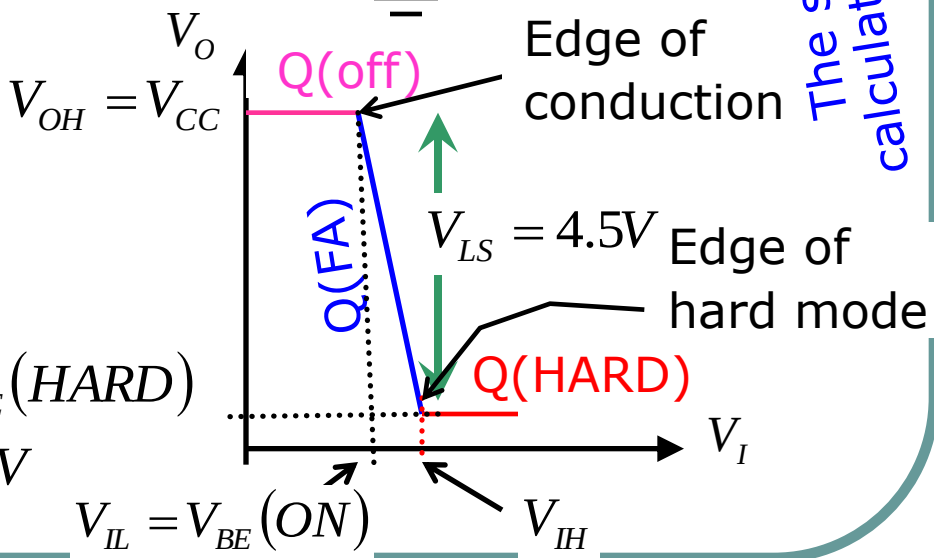
$V_{OL} = V_{CE}(HARD) = 0.5V$

Logic swing voltage=

$V_{LS} = V_{OH} - V_{OL} = 4.5V$

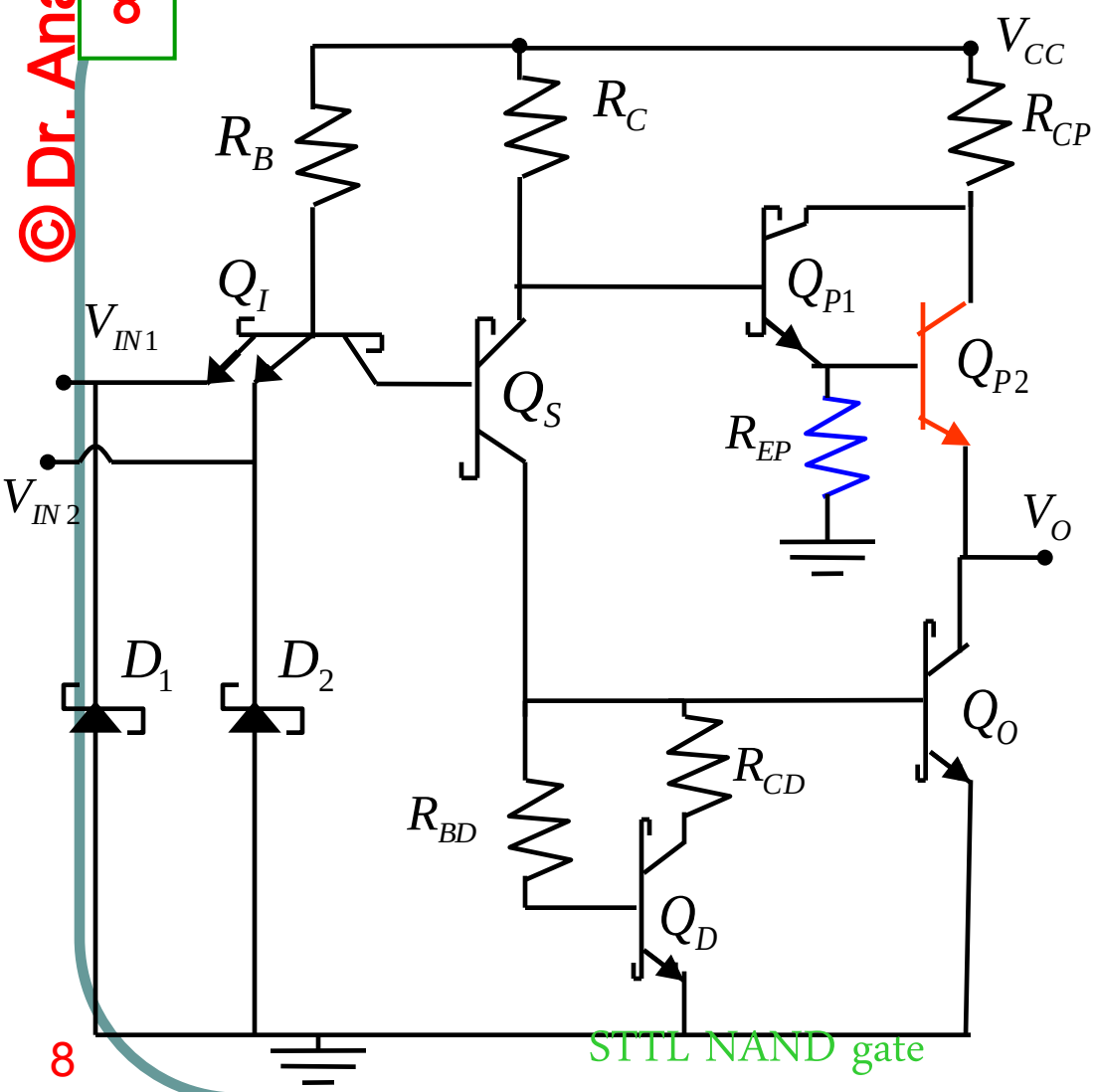
$V_{OL} = V_{CE}(HARD)$

$= 0.5V$



The slope will be calculated in the class

Schottky-Clamped TTL (SSTTL) 54S00/74S00



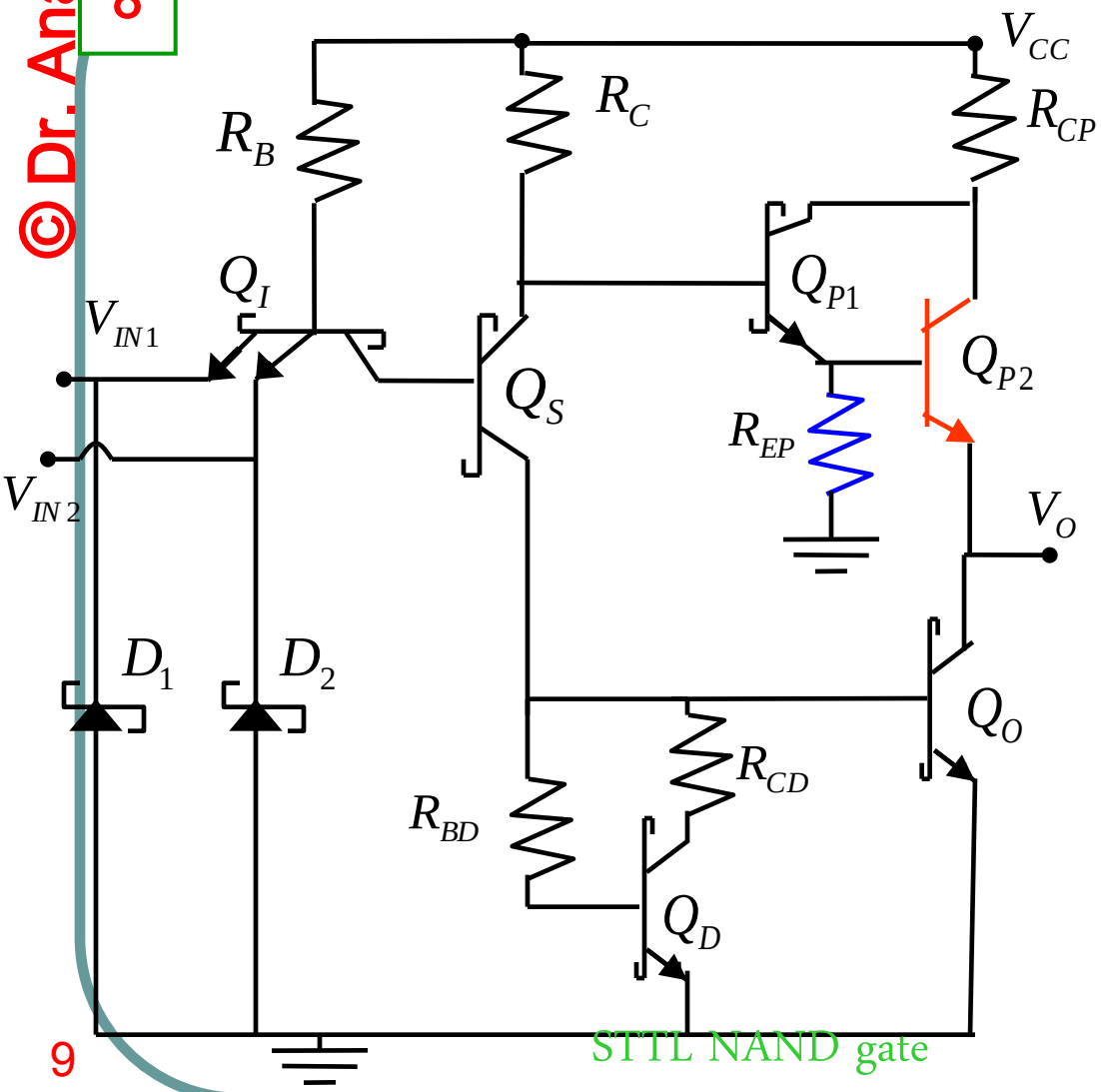
STTL NAND gate

- BJTs are replaced with SBJTs (except for Q_{P2})
- The Darlington pair (Q_{P1} & Q_{P2}) provides higher current to charge the load capacitance (Output low-high)
- Q_{P2} is a normal BJT because it can not saturate since

$$V_{CE,P2}(FA) = V_{CE,P1}(HARD) + V_{BE,P2}(FA)$$

$$V_{CE,P2}(FA) > V_{CE}(sat)$$

Schottky-Clamped TTL (SSTTL) 54S00/74S00



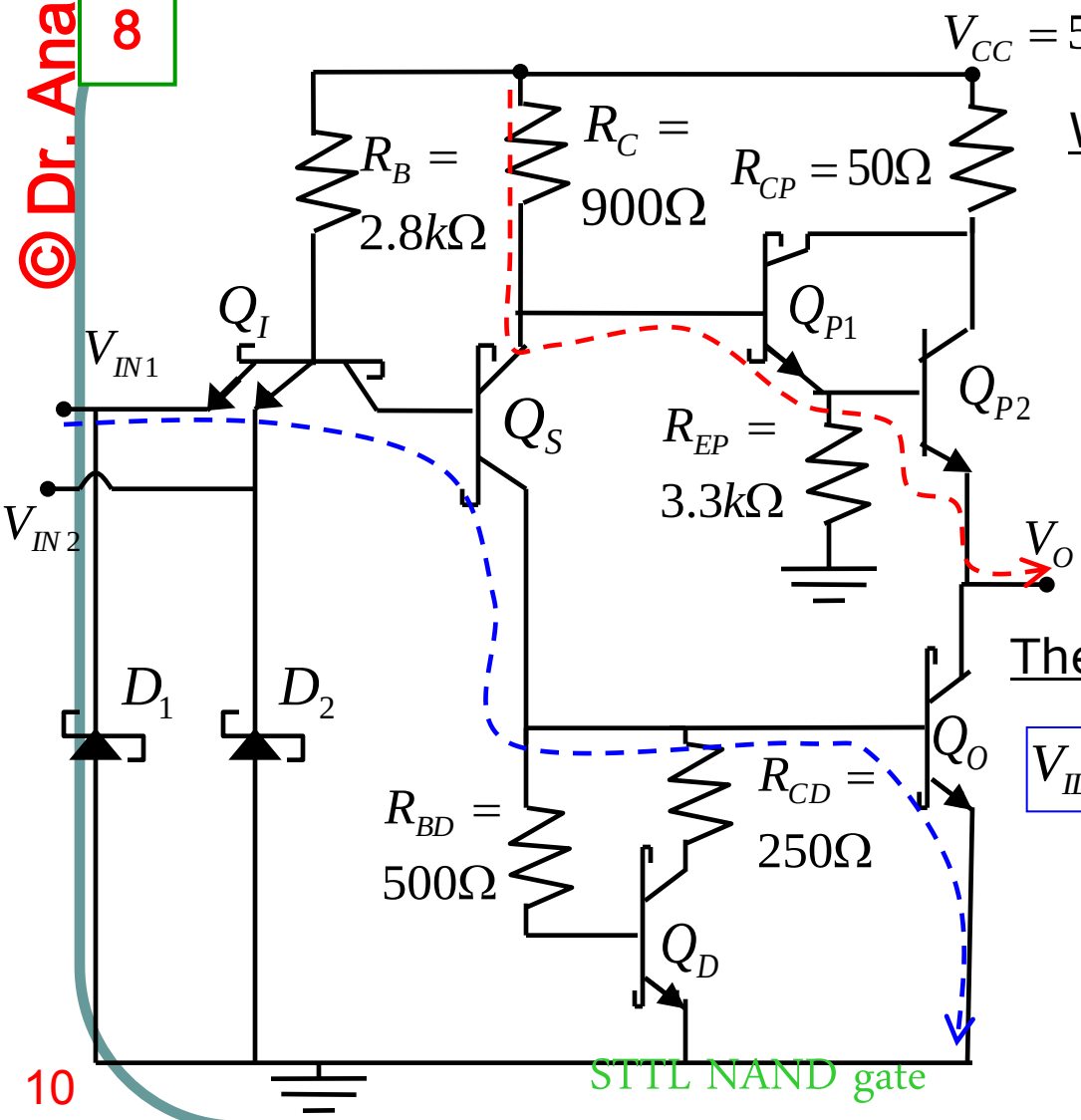
STTL NAND gate

Advantages of Q_D, R_{BD}, R_{CD}:

1. The break point between V_{OH} and V_{OL} is eliminated (Q_S, Q_O turn ON at the same time)
2. Narrower transition width and better noise margin
3. Discharge the base charge of Q_O during the low-high transition

R_B, R_C have smaller values than in TTL gates to increase the fan-out (but also increase $P_{CC}(avg)$)

VTC of SSTTL



STTL NAND gate

V_{OH}

When V_{IN} is low: Q_I is „Hard".

Q_S , Q_D, and Q_O are off.

Q_{P1} and Q_{P2} are ON.

$$V_{OH} = V_{CC} - V_{BE,P1}(FA) - V_{BE,P2}(FA)$$

$$V_{OH} = 5 - 1.4 = 3.6V$$

(Neglecting I_{BP}.)

V_{IL}

The necessary voltage to turn Q_O ON

$$V_{IL} = -V_{CE}(HARD) + V_{BE,S}(FA) + V_{BE,O}(FA$$

$$V_{IL} = -0.5 + 1.4 = 0.9V$$

VTC of SSTTL

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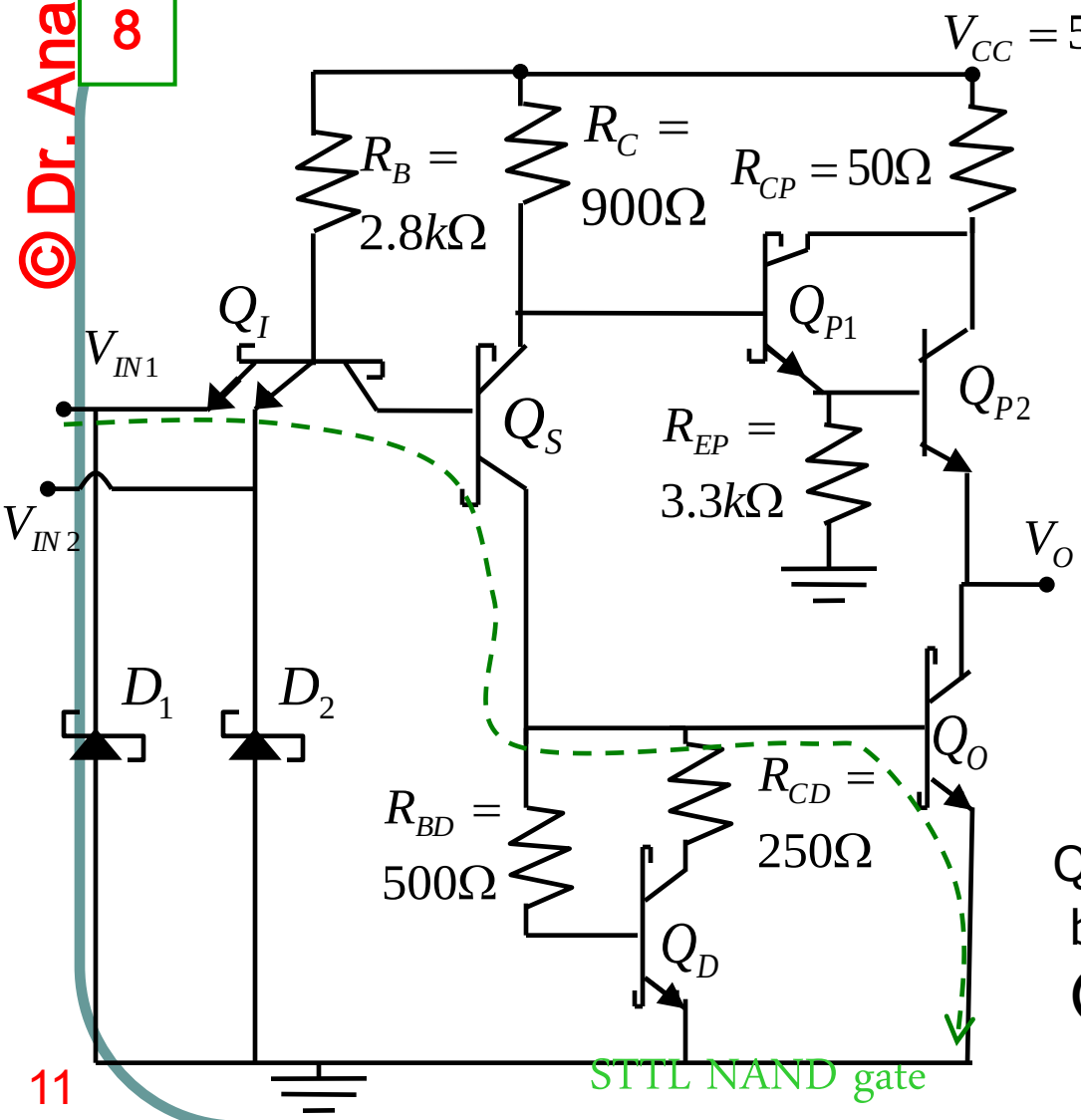


STTL NAND gate

V_{IH} Q_S , and Q_O are in on-hard mode.

$$V_{IH}=-V_{CE}(HARD)+V_{BE,S}(HARD)+V_{BE,O}(HARD)$$

$$V_{IH}=-0.5+1.6=1.1V$$

V_{OL} Q_O is SBJT

$$V_{OL}=V_{CE,O}(HARD)=0.5V$$

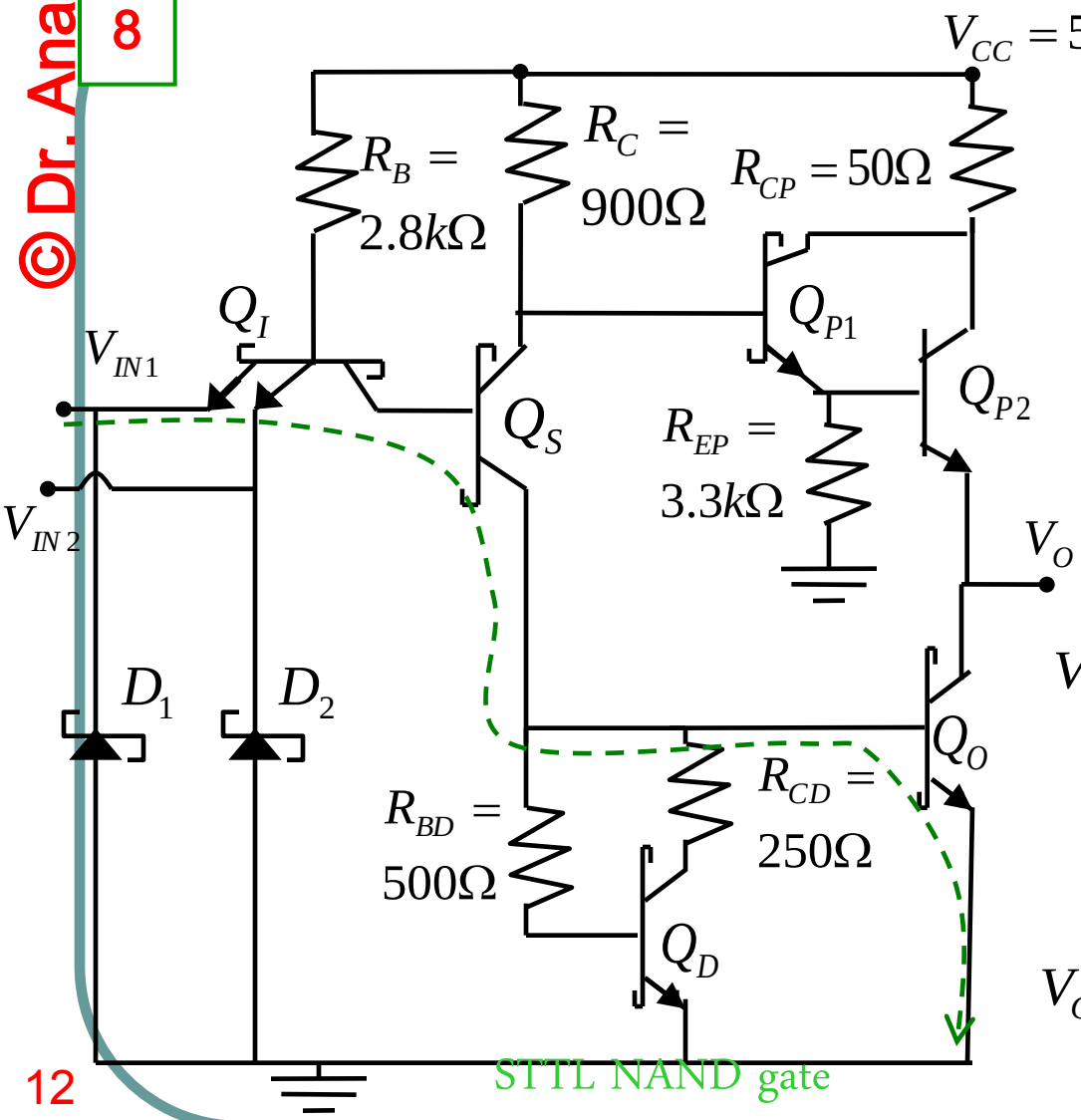
$$V_{B,P1}=V_{CE,S}(HARD)+V_{BE,S}(HARD)$$

$$V_{B,P1}=1.3>0.7V$$

Q_{P1} is ON through R_{EP} but Q_{P2} is OFF

($V_{BE,P2}=1.3-0.7-0.5=0.1V<V_{BE}(FA)$)

VTC of SSTTL



STTL NAND gate

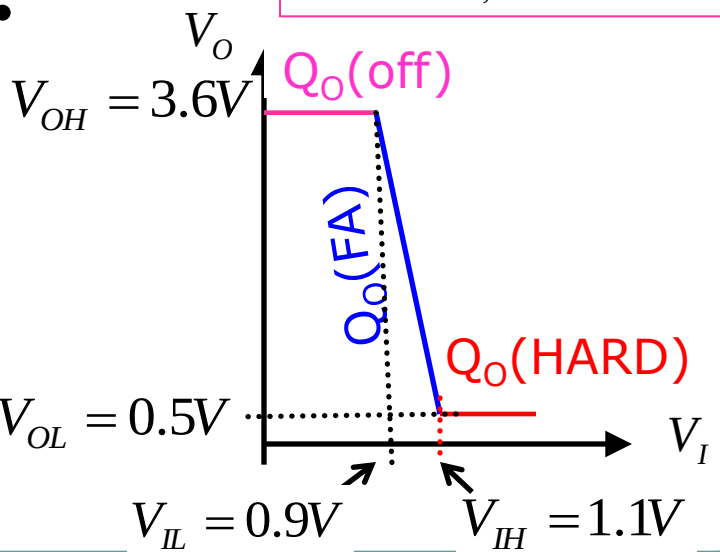
V_{IH} Q_S , and Q_O are in on-hard mode.

$$V_{IH} = -V_{CE}(HARD) + V_{BE,S}(HARD) + V_{BE,O}(HARD)$$

$$V_{IH} = -0.5 + 1.6 = 1.1V$$

V_{OL} Q_O is SBJT

$$V_{OL} = V_{CE,O}(HARD) = 0.5V$$



Fan-Out of SSTTL

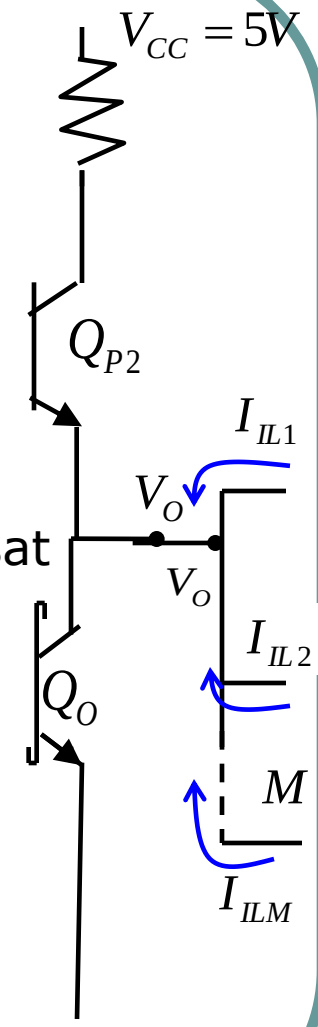
Ch 8

When the output is high, I_{IL} is negligible.
Therefore, Fan-out depends on the output low state

$$M = \frac{I_{OL}}{I_{IL}}$$?

Input current low I_{IL}

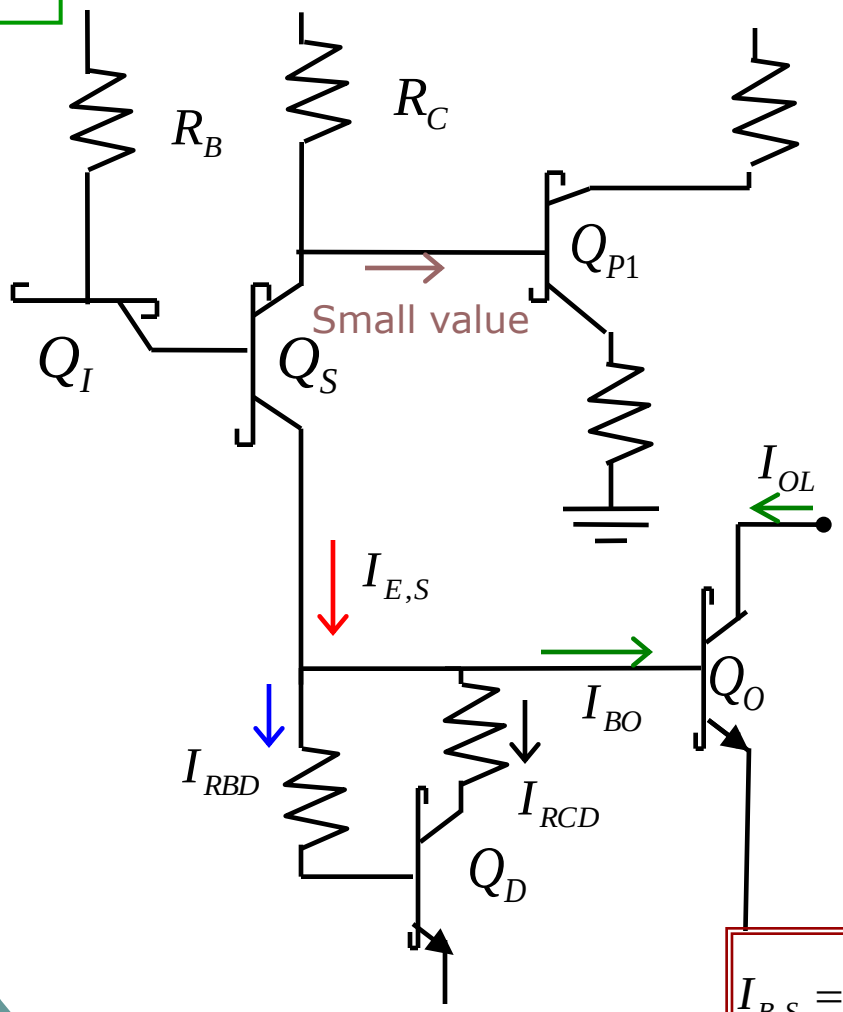
For the input low state, Q_I is sat and Q_S is cut-off



$$I_{IL} = I_{EI} = I_{RB} = \frac{V'_{CC} - V'_{BE,I}(HARD) - V_{CE,O}(HARD)}{R'_B}$$

Fan-Out of SSTTL

Ch 8



Output current low I_{OL}

$$I_{OL} = I_{C,O}(HARD)$$

Since the output Q_{P2} is cut-off

$$I_{OL} = \beta_F I_{BO}$$

$$I_{BO} = I_{E,S} - (I_{RBD} + I_{RCD})$$ Negligible

$$I_{RCD} = \frac{V_{BE,O}(HARD) - V_{CE,D}(HARD)}{R_{CD}}$$

$$I_{E,S} = I_{B,S} + I_{C,S}$$

$$I_{C,S} = \frac{V_{CC} - V_{CE,S}(HARD) - V_{BE,O}(HARD)}{R_C}$$

$$I_{B,S} = \frac{V_{CC} - V_{BC,I}(HARD) - V_{BE,S}(HARD) - V_{BE,O}(HARD)}{R_B}$$

Fan-Out of SSTTL

Ch 8

- Example

Determine the maximum fan-out of the SBJT circuit shown, assuming $\beta_F=49$

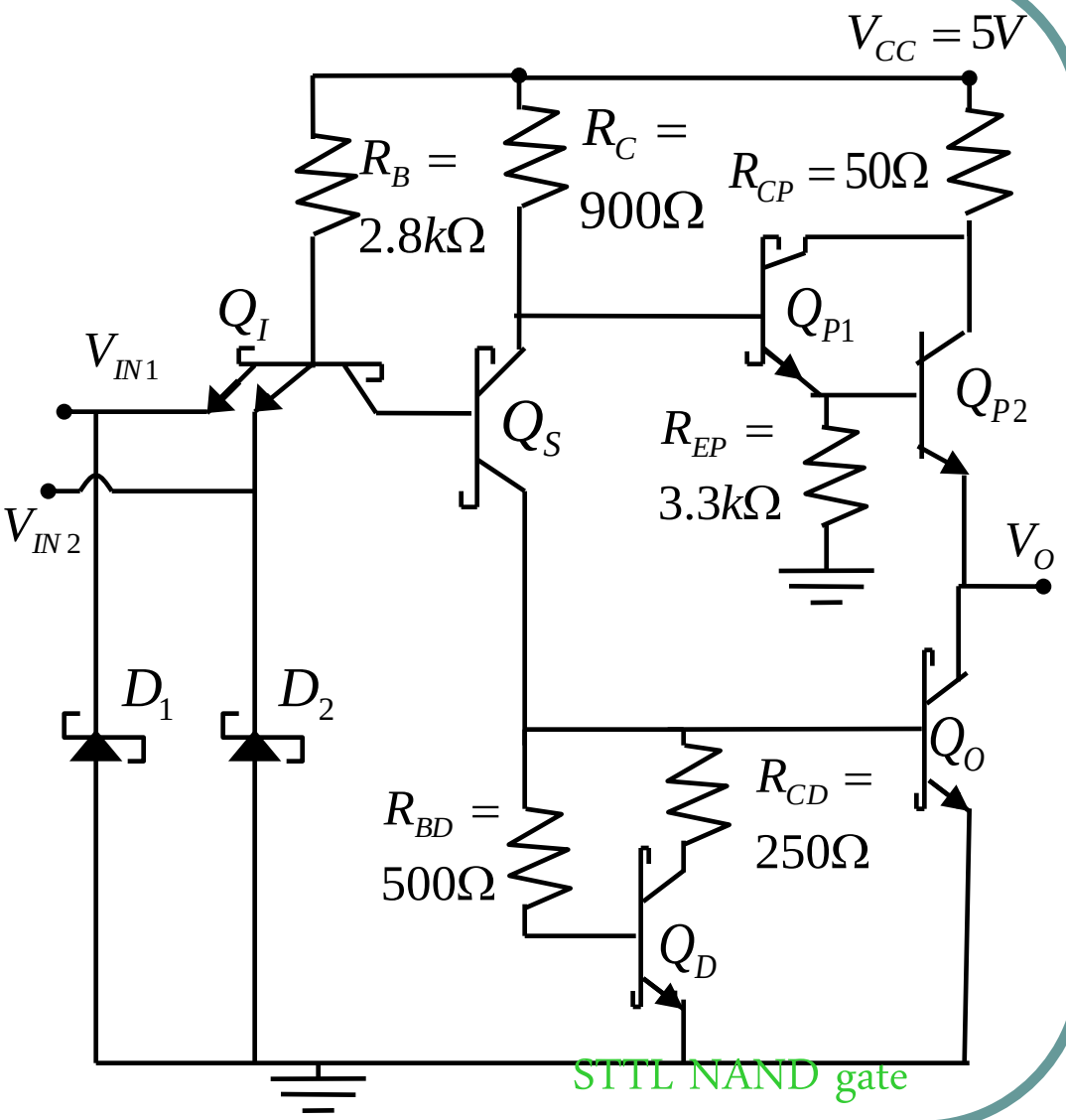
- Solution

$$I_{IL}=\frac{5-0.8-0.5}{2.8k}=1.32mA$$

$I_{RCD}=1.2mA$ $\quad$ $I_{B,S}=1.11mA$

$I_{C,S}=4.11mA$

$\boxed{M=149}$



STTL NAND gate

- HW #8:Solve Problems:8.1 , 8.3, 8.8, and 8.19