# CHAPTER SEVEN

# Transistor- Transistor logic (TTL)

Digital Electronics.

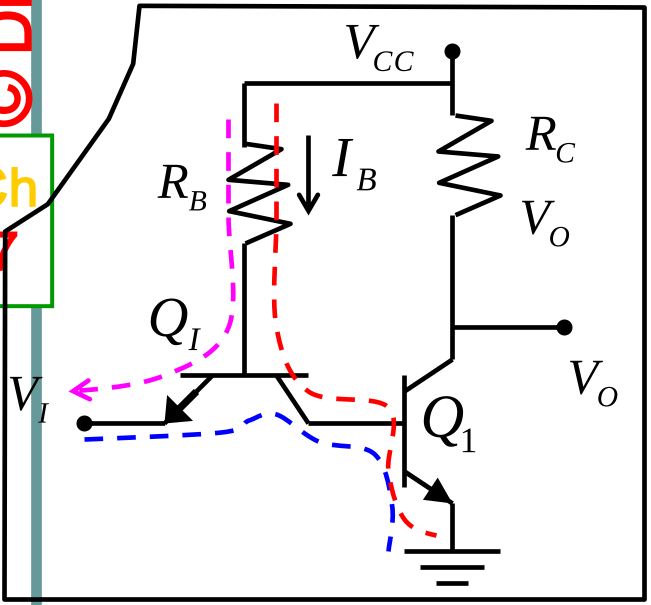
# Introduction

**Diode-Transistor Logic** → **Transistor-Transistor Logic**

The TTL circuits provide

1. Increased fan-out.
2. Improved transient response.
3. Reduction in chip area.
4. Inclusion of an active pull-up circuits

# Basic TTL Inverter



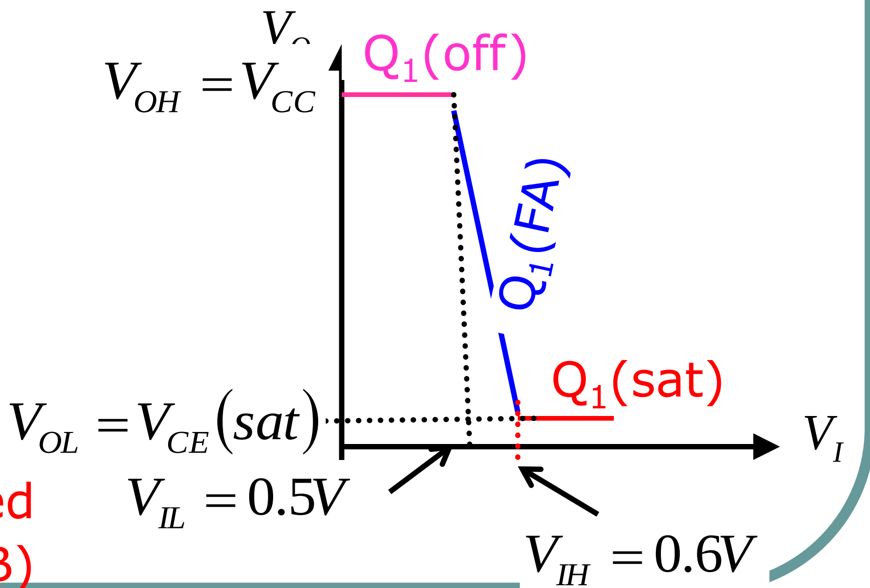
For $\begin{cases} V_I \le V_{IL} = V_{BE,1}(FA) - V_{CE,I}(sat) \\ I_B = \dfrac{V_{CC} - V_{BE,I} - V_I}{R_B} \\ V_{BE,1} = V_{CE,I}(sat) + V_{IL} \end{cases}$

→ BE of $Q_I$ is forward-biased

For typical values of $R_B$, $I_B$ is in mA, $Q_I$ is sat.

$Q_1$ is cut-off $\boxed{V_{OH} = V_{CC}}$

For $\{ V_I \ge V_{IL}$ → $Q_I$ is sat& $Q_1$ is FA

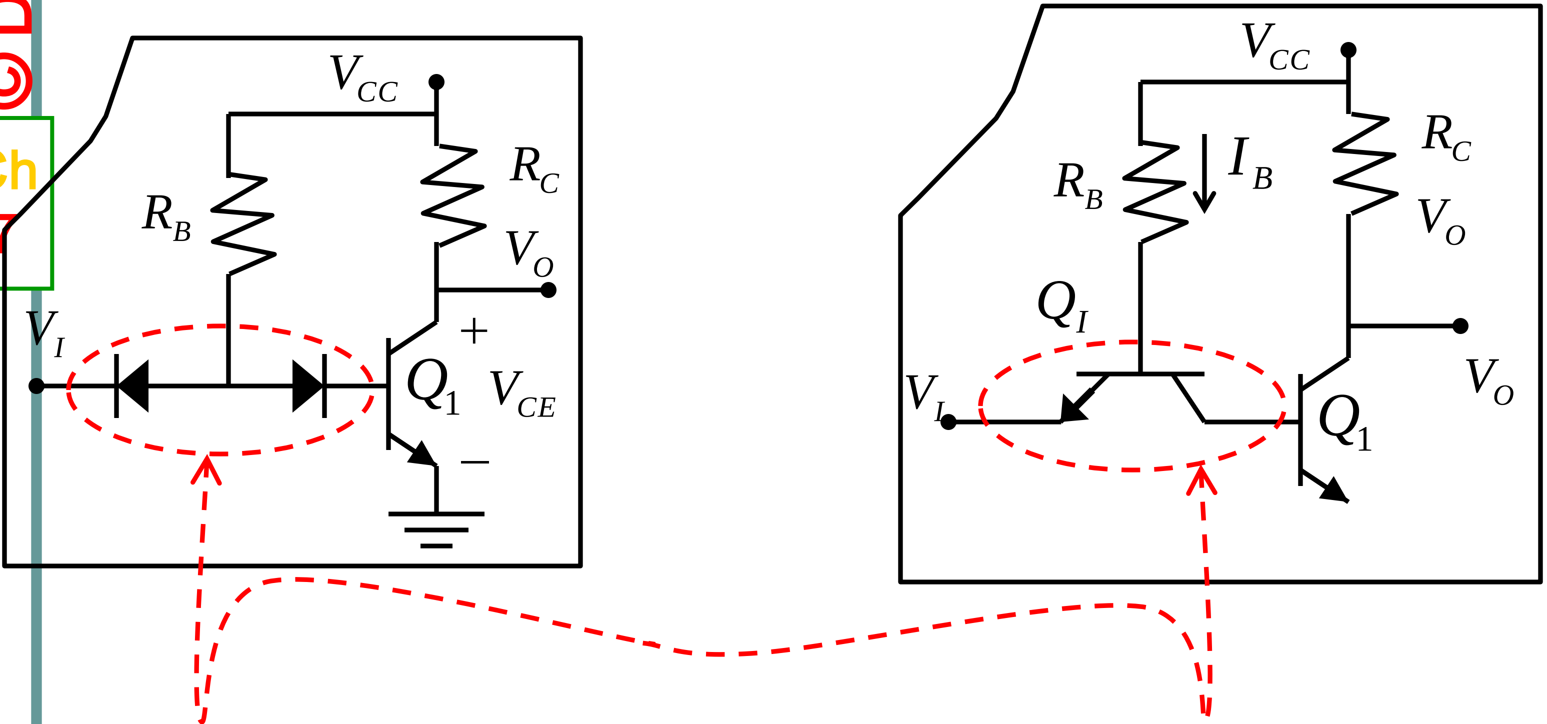


For $\begin{cases} V_I = V_{IH} = V_{BE,1}(sat) - V_{CE,I}(sat) \\ \boxed{V_{OL} = V_{CE}(sat)} \end{cases}$ → $Q_1$ is sat

For $V_I > V_{IH}$ BE of $Q_I$ is reverse-biased

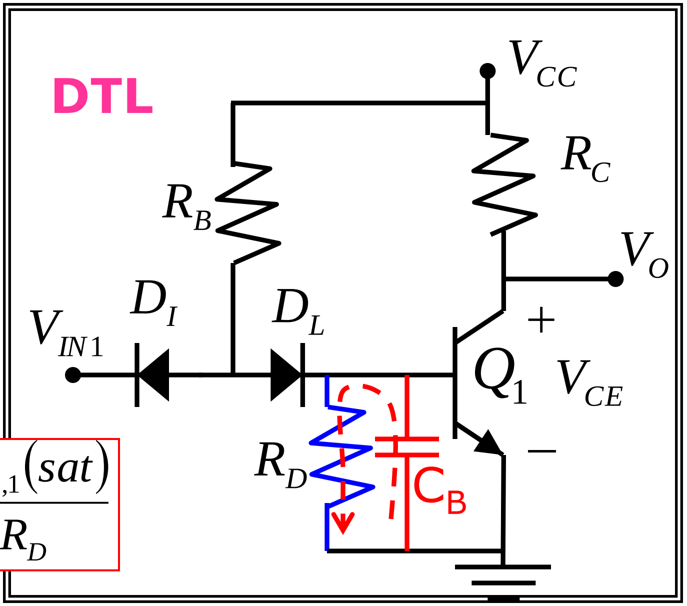
Inverse-active mode (RB)

# Basic TTL Inverter

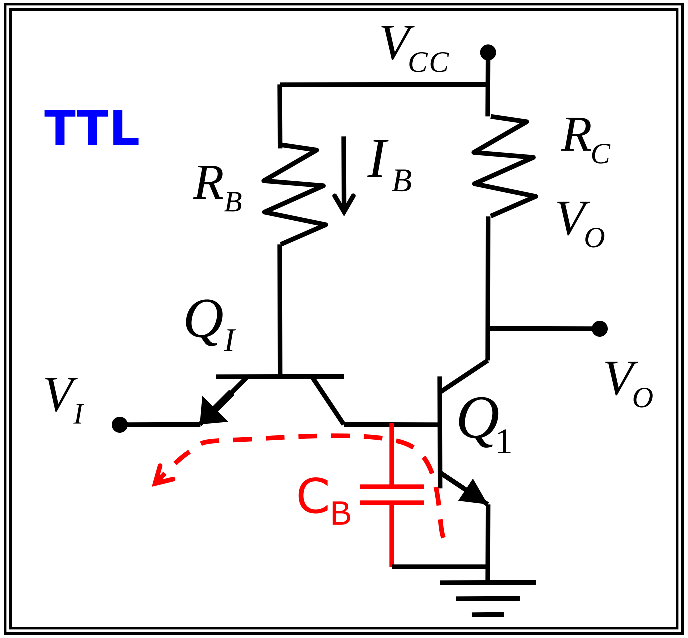


- The input and level-shifting diodes are replaced by $Q_I$
- The $Q_I$ BJT requires less area than the two diodes

# Stored-Charge Removal in TTL cct's



$$I_{SCR} = \frac{V_{BE,1}(sat)}{R_D}$$



When $V_I$ changes from High ($V_{IH}$) to Low ($V_{IL}$), $Q_1$ is switched from saturation to cut-off, the stored base charges in $C_B$ must be removed.

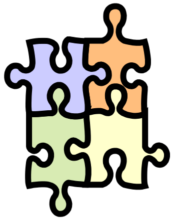
$$V_{C,I} = V_{C_B} = V_{BE,1}(sat) \quad V_{BC,I} = V_{B,I} - V_{C,I} = V_{BE,I}(FA) + V_{IL} - V_{BE,1}(sat) \rightarrow V_{BC,I} \cong 0.1V$$

BC junction of $Q_I$ is slightly forward-biased but insufficient to saturate $Q_I$ → $Q_I$ is **F.A**.

$$I_{C,I} = \beta_F\left(\frac{V_{CC} - V_{BE,I}(FA) - V_{CE,1}(sat)}{R_B}\right)$$

Discharge current $I_{C,I}$

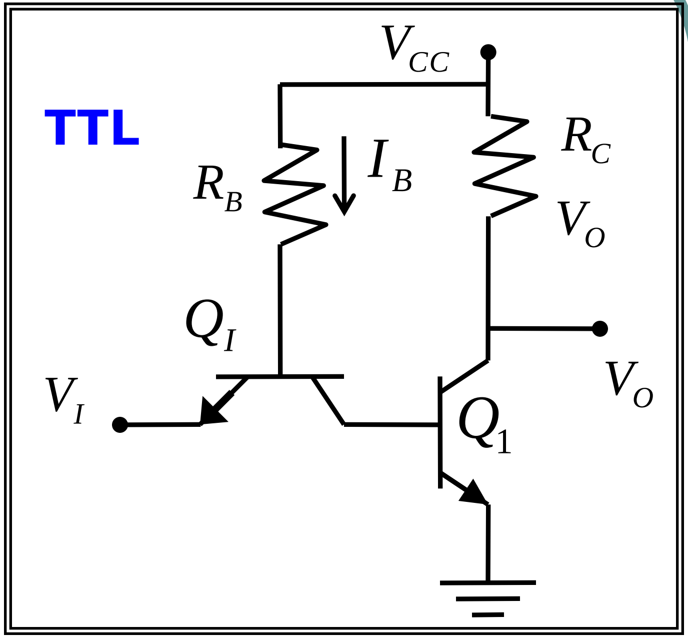
# Stored-Charge Removal in TTL cct's



- Example

Calculate the improvement factor in stored charge removal for TTL over DTL circuits assuming:

$V_{CE}(sat)=0.2V$, $V_{BE}(FA)=0.7V$, $V_{BE}(sat)=0.8V$, $V_{CC}=5V$, $R_B=2k\Omega$, $R_D=5k\Omega$, and $\beta_F=50$.



- Solution

In DTL $$I_{SCR}=\frac{V_{BE,1}(sat)}{R_D}=\frac{0.8}{5}=0.16mA$$

In TTL $$I_{C,I}=\beta_F\left(\frac{V_{CC}-V_{BE,I}(FA)-V_{CE,1}(sat)}{R_B}\right)=50\left(\frac{5-0.7-0.2}{2}\right)$$

$$I_{C,I}=102.5mA$$

Improvement factor= 640.6

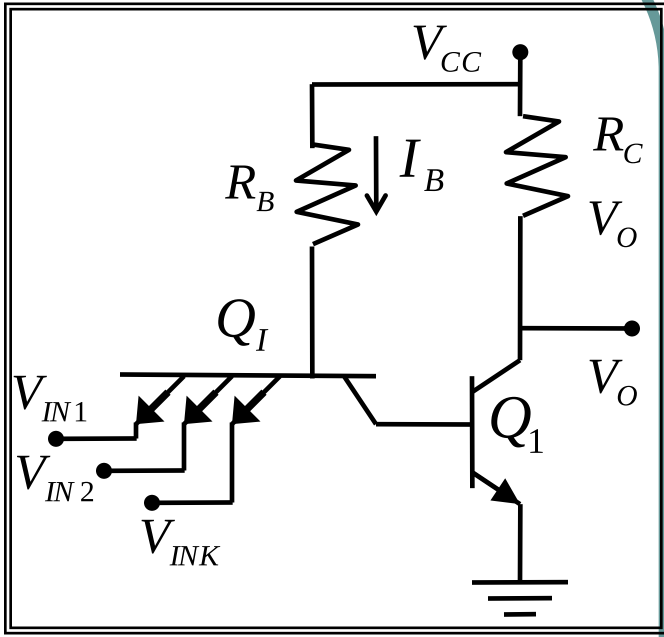
# Basic TTL NAND Gate

If at least one input is less than $V_{IL}$, then the $Q_1$ is off.

$$V_{OH} = V_{CC}$$

If all inputs are greater than $V_{IH}$, then the $Q_1$ is sat.

$$V_O = V_{CE}(sat)$$



Multiple-emitter BJT requires much less chip area than using individual transistors for each input

# Standard TTL NAND Gate With Totem Pole Output

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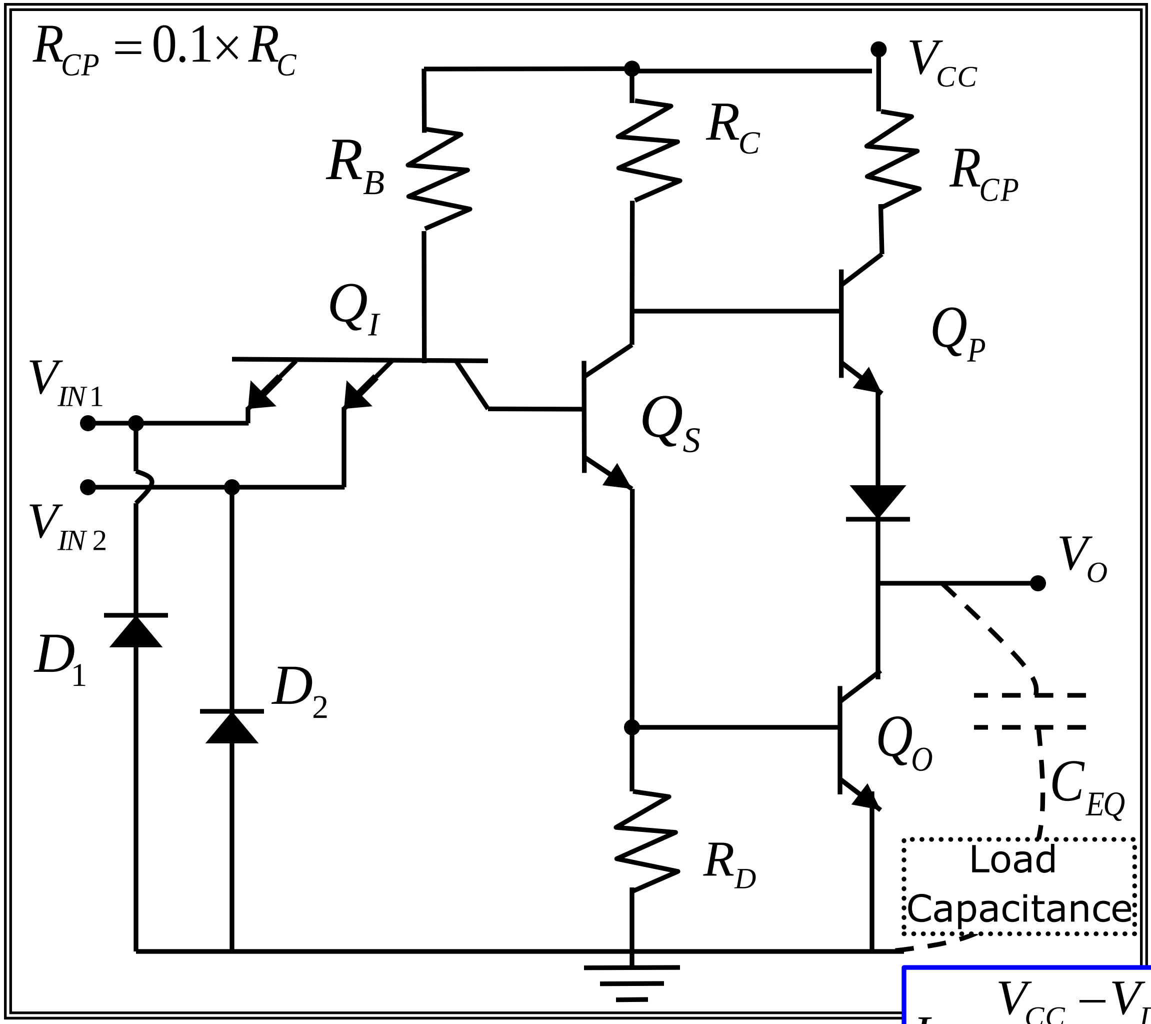
Ch 7



In basic TTL: $C_{EQ}$ is charged through $R_C$

$$\tau = R_C \times C_{EQ}$$

Initial charge current

$$I_i = \frac{V_{CC} - V_{CE}(sat)}{R_C}$$

In standard TTL: $C_{EQ}$ is charged through $R_{CP}$

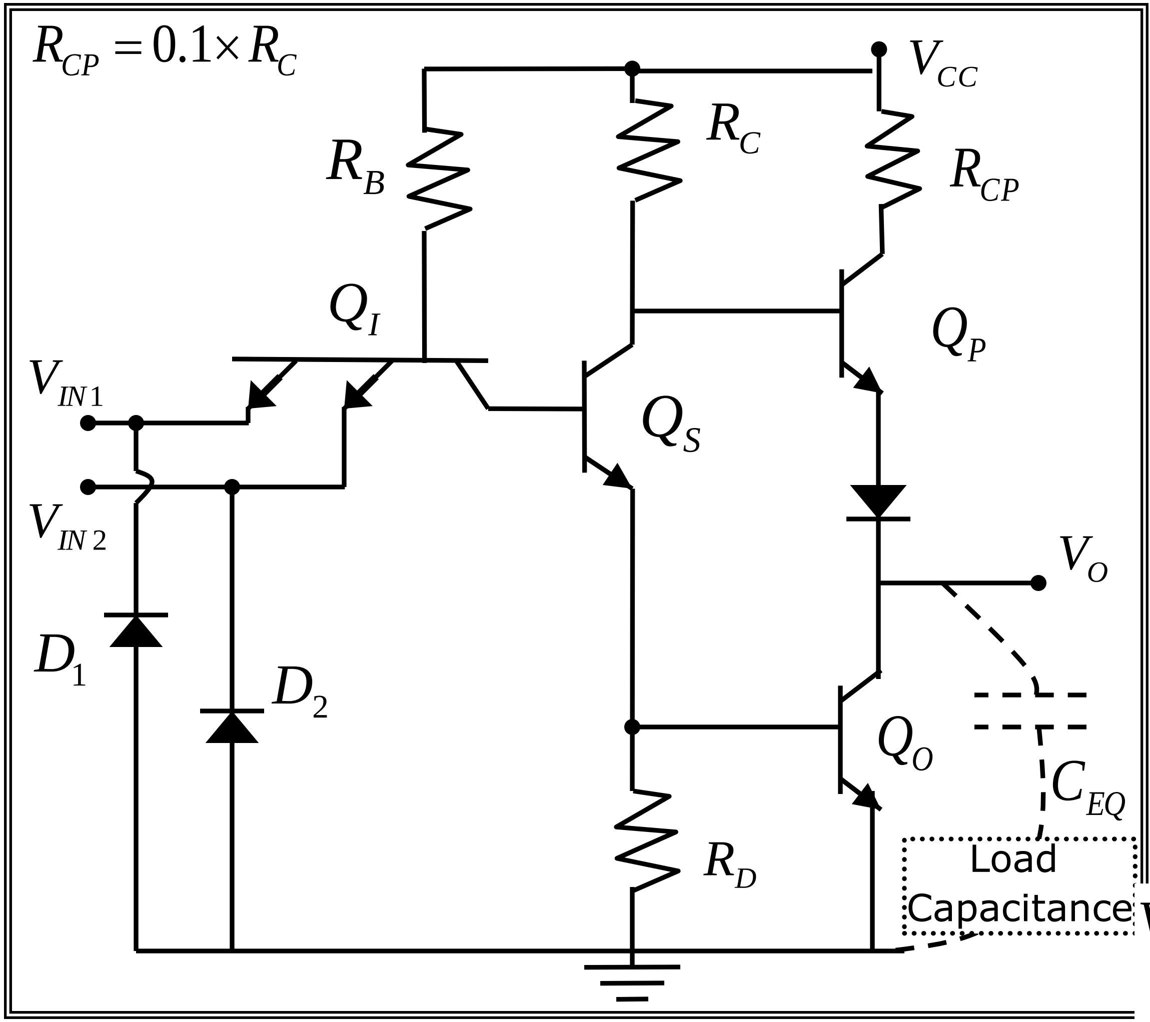
$$\tau = R_{CP} \times C_{EQ}$$

Initial charge current

$$I_i = \frac{V_{CC} - V_D(ON) - V_{CE,P}(sat) - V_{CE,O}(sat)}{R_{CP}}$$

Since $R_{CP} << R_C$, standard TTL has much smaller rise time

# Standard TTL NAND Gate With Totem Pole Output



**Function of $Q_S$:**

It is a driver splitter

- Provides base-current to $Q_O$
- Pull-down of $Q_P$.
- Shifts the transition region of VTC from (0.5-0.6)V to (1.2-1.4)V to enhance the noise margin

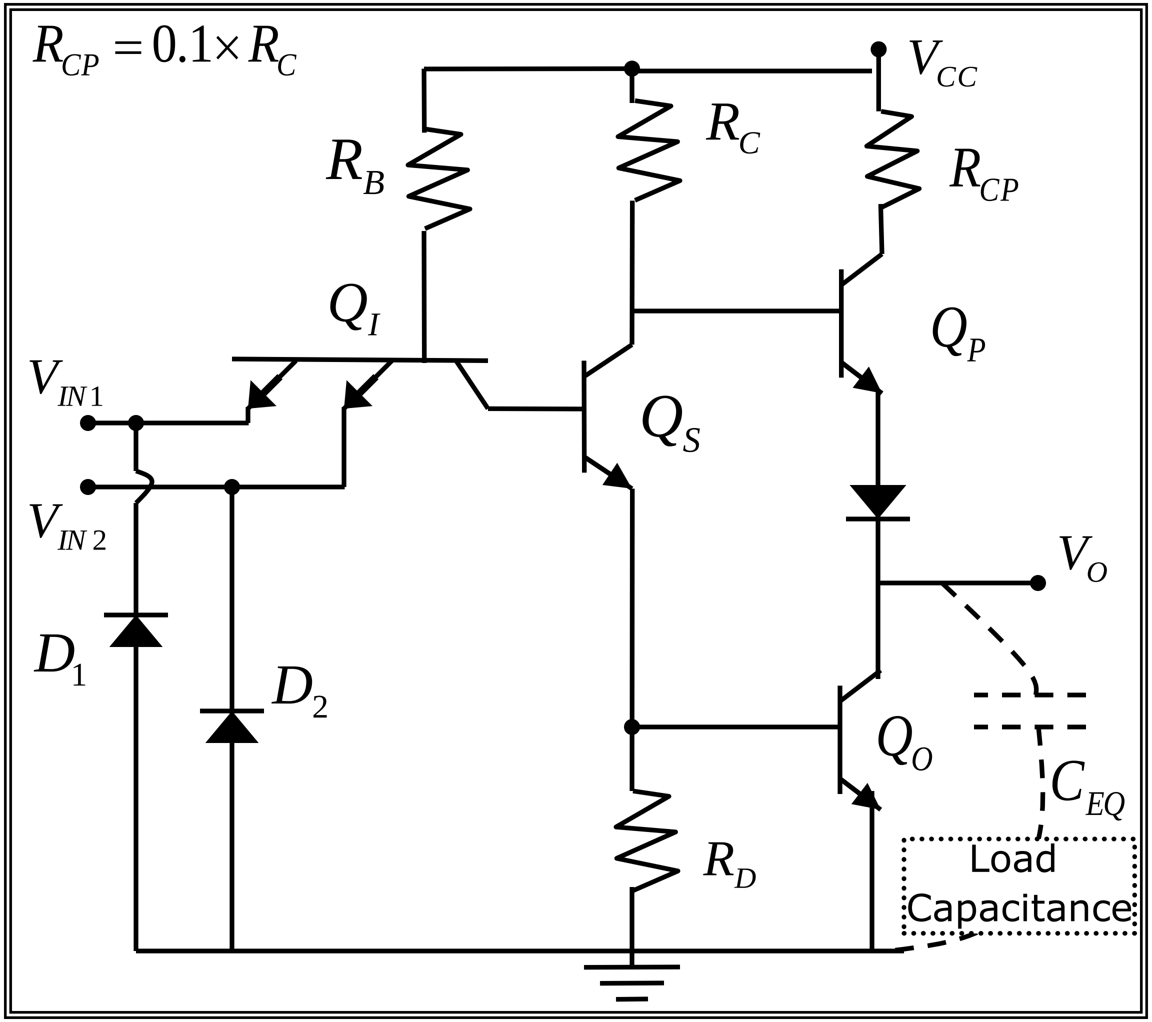
$Q_S$ drives only either $Q_P$ **(FA)** or $Q_O$ into sat

When $Q_O$ is sat, $Q_S$ is also sat, and

$$V_{BE,P} = \cancel{V_{CE,S}(sat)} + V_{BE,O}(sat) - V_D(ON) - \cancel{V_{CE,O}(sat)}$$

$Q_P$ is cut-off

# Standard TTL NAND Gate With Totem Pole Output

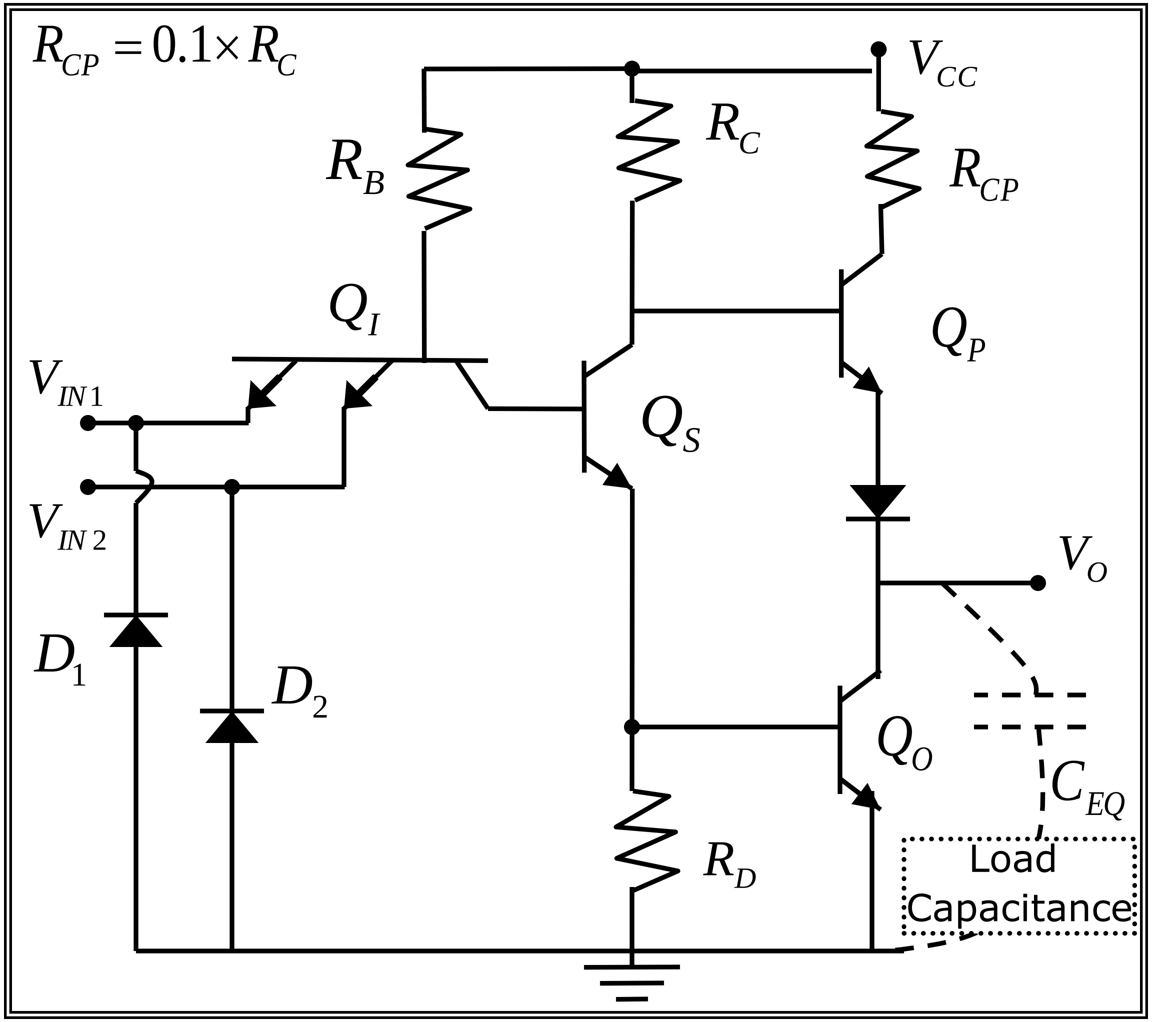


**Function of $R_D$:**

In basic TTL, the stored charge of $Q_O$ is removed by $Q_I$.

In STTL, $Q_I$ no longer sinks the base current of $Q_O$, Therefore, this removal is done by $R_D$ since $Q_O$ is not heavily sat.

# Standard TTL NAND Gate With Totem Pole Output



**Function of $D_1$ & $D_2$:**

The clamping diodes are used to limit the negative swing of the input voltages to <u>one diode drop</u> below ground

# Standard TTL VTC

$\underline{V_{OH}}$

When $V_{IN}$ is low:

$$I_{B,I} = \left( \frac{V_{CC} - V_{BE,I}(sat) - V_{IL}}{R_B} \right)$$

The collector current $I_{CI}$ of $Q_I$ is

$$I_{C,I} = -I_{B,S(SCR)} << \beta_F I_{B,I}$$

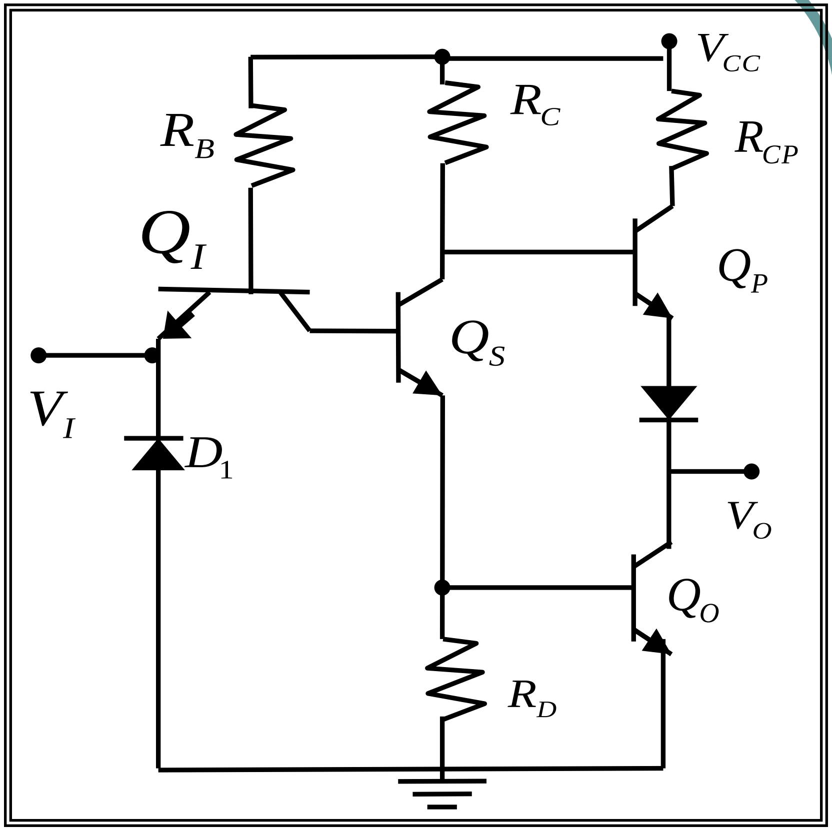
Therefore, $Q_I$ is sat.

$$V_{B,S} = V_{IL} + V_{CE,I}(sat) < V_{BE,S}(FA)$$

$Q_S$ and $Q_O$ are off.

$$\boxed{V_{OH} = V_{CC} - V_{BE,P}(FA) - V_D(ON)}$$

(Neglecting $I_{BP}$.)



$$I_{BP,I} = \frac{V_{CC} - V_{BE,P}(FA) - V_D(ON)}{R_C + (1+\beta_F) \times R_M}$$

$\approx 10M\Omega$

# Standard TTL VTC

$\underline{V_{IL}}$

As $V_I$ increases to :

$$V_I = -V_{CE,I}(sat) + V_{BE,S}(FA)$$

$Q_s$ starts conducting

$$V_{IL} = V_{BE,S}(FA) - V_{CE,I}(sat)$$

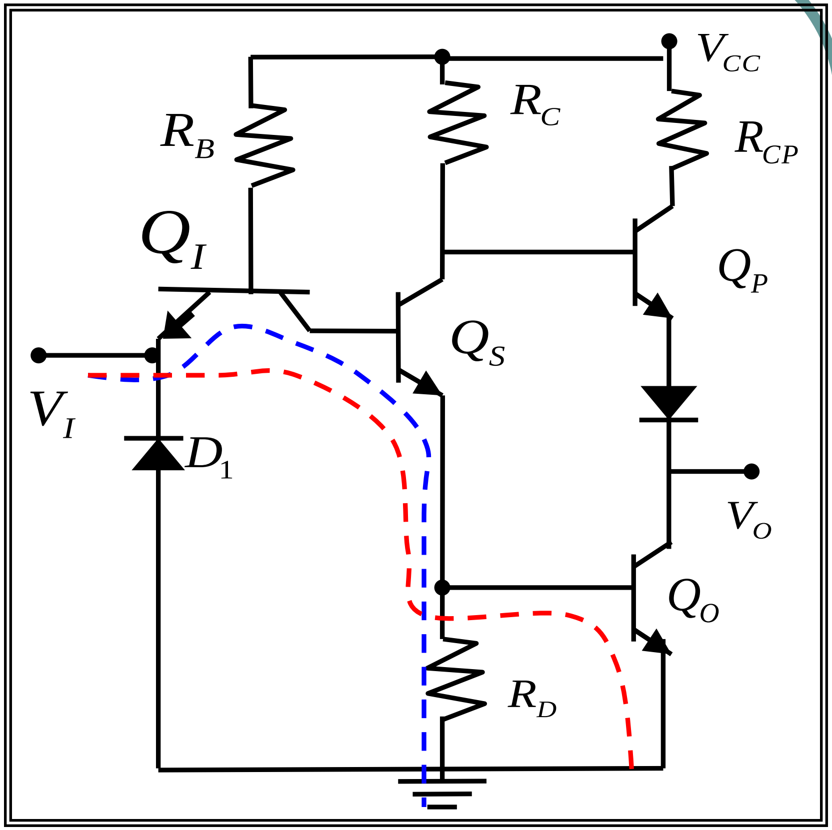
→ $Q_I$ & $Q_S$ are ON, $Q_O$ is OFF

As $V_I$ increases further to :

$$V_I = -V_{CE,I}(sat) + V_{BE,S}(FA) + V_{BE,O}(FA)$$

$Q_O$ becomes FA

$$V_{IB} = 2V_{BE}(FA) - V_{CE,I}(sat)$$



$V_{IB}$ is called Input Breakpoint Voltage

$V_{OB}$ is the output voltage that corresponds $V_{IB}$ can be found just as $Q_O$ turns ON.

$$I_{RC} = I_{RD} = \frac{V_{BE,O}(FA)}{R_D} \Rightarrow V_{OB} = V_{CC} - R_C I_{RC} - V_{BE,P}(FA) - V_D(ON)$$

# Standard TTL VTC

$V_{IH}$

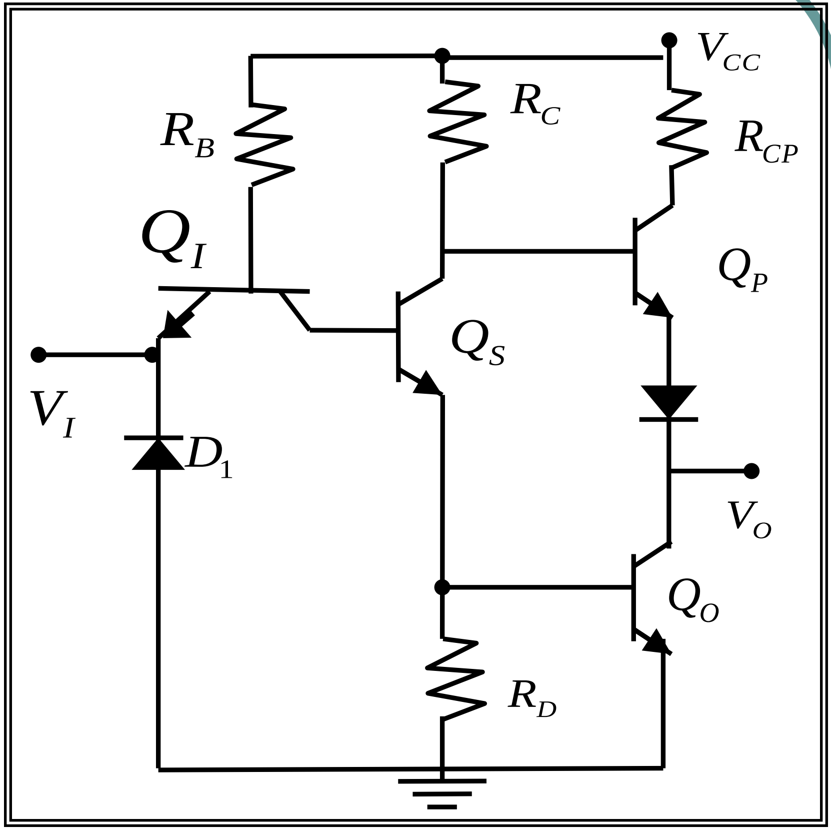
Q$_O$ and Q$_S$ are sat when

$$V_I = -V_{CE,I}(sat) + V_{BE,S}(sat) + V_{BE,O}(sat)$$

$$V_{IH} = 2V_{BE}(sat) - V_{CE,I}(sat)$$

$$V_{IL} = V_{BE,S}(FA) - V_{CE,I}(sat)$$

$$V_{OL} = V_{CE,O}(sat)$$

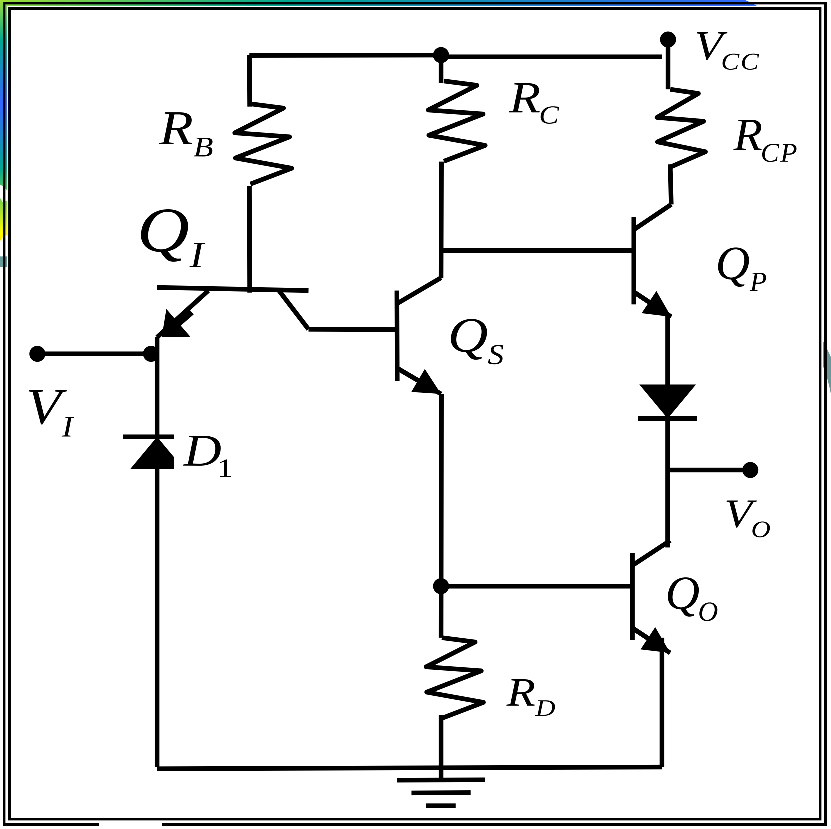


# Standard TTL VTC

- **Example**

Plot the VTC of standard TTL circuits assuming:

$V_{CE}(sat)=0.2V$, $V_{BE}(FA)=0.7V$, $V_{BE}(sat)=0.8V$, $V_{CC}=5V$, $R_B=4k\Omega$, $R_C=1.6k\Omega$, $R_{CP}=100\Omega$, $R_D=1k\Omega$, and $\beta_F=100$.



- **Solution**

$$V_{OH}=5-1.4=3.6V$$

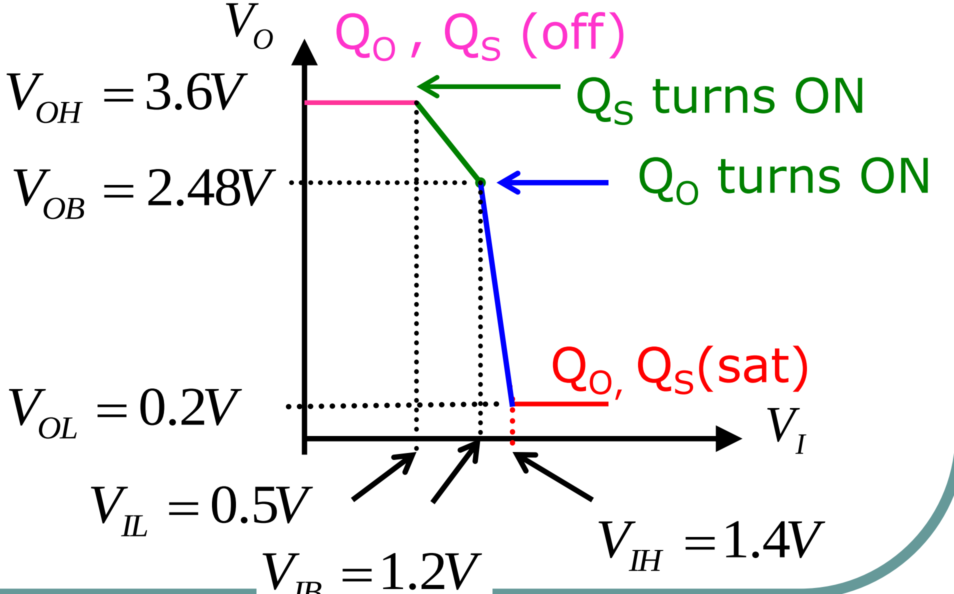
$$V_{IL}=-0.2+0.7=0.5V$$

$$V_{IB}=-0.2+1.4=1.2V$$

$$V_{OB}=5-\frac{0.7}{1}\times1.6-1.4$$

$$=2.48V$$

$$V_{OL}=0.2V$$



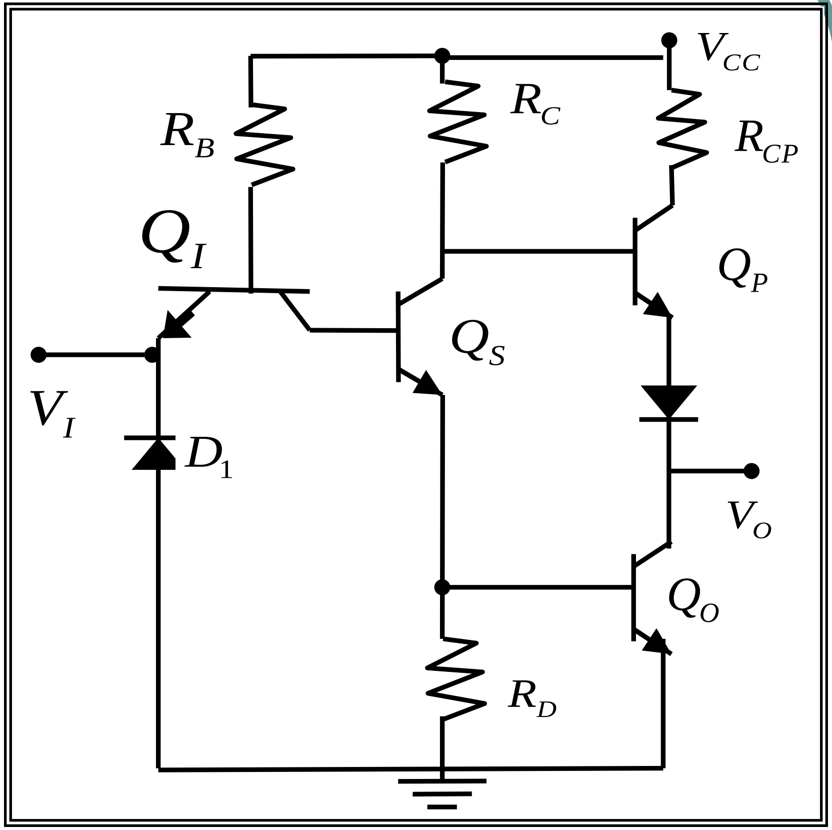
# TTL SPICE Simulation

- Example

*Repeat the last example using PSPICE

*Plot $V_O$ as a function of $V_I$

*Refer to pages 93-94 in the text book.



# TTL Fan-Out

When the output is high, $I_{IL}$ is negligible.
Therefore, Fan-out depends on the output low state

$$M = \frac{I_{OL}}{I_{IL}}$$

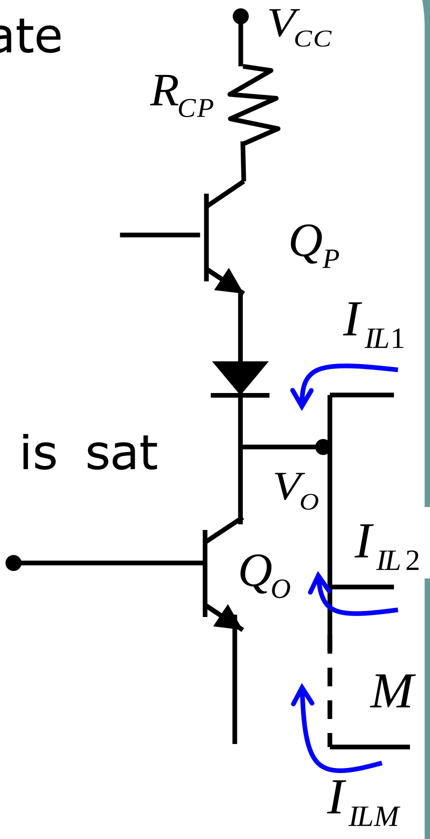
?

**Input current low $I_{IL}$**

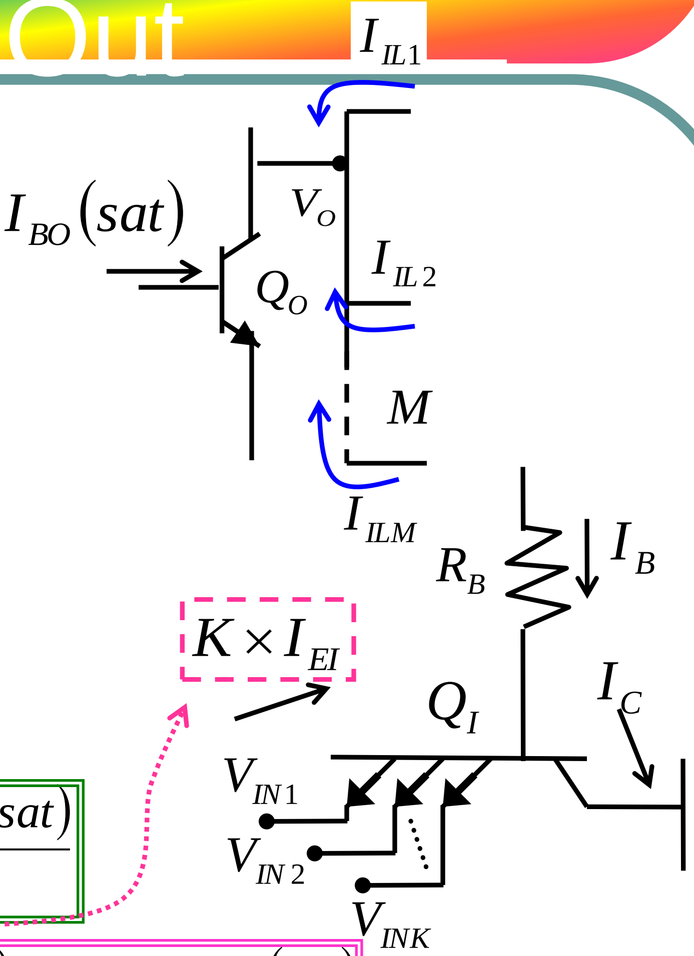
For the input low state, $Q_I$ is sat and $Q_S$ is cut-off

$$I_{CI} = -I_{BS} \left(\cong 0\right)$$

$$\boxed{I_{IL} = I_{EI} = I_{RB} = \frac{V'_{CC} - V'_{BE}\left(sat\right) - V_{CE,O}\left(sat\right)}{R'_B}}$$



# TTL Fan-Out



**Output current low $I_{OL}$**

$$I_{OL}=I_{C,O}(sat)$$

Since the output $Q_P$ and $D_L$ are cut-off

$$I_{OL}=\sigma_{OL}\beta_F I_{BO}(sat)$$

$$\boxed{I_{BO}=I_{ES}(sat)-\frac{V_{BE,O}(sat)}{R_D}}$$

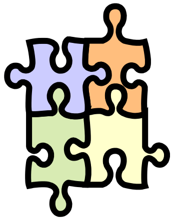
$$\boxed{I_{ES}(sat)=I_{CS}(sat)+I_{BS}(sat)}$$

$$\boxed{I_{CS}(sat)=\frac{V_{CC}-V_{CE,S}(sat)-V_{BE,O}(sat)}{R_C}}$$

$$\boxed{I_{CI}(RA)=I_{BS}(sat)=I_{BI}(RA)+K\times I_{EI}(RA)=I_{BI}(RA)+\beta_R\times K\times I_{BI}(RA)}$$

$$\boxed{I_{BS}(sat)=(1+K\times\beta_R)\times I_{BI}=(1+K\times\beta_R)\times\left(\frac{V_{CC}-V_{BC,I}(RA)-V_{BE,S}(sat)-V_{BE,O}(sat)}{R_B}\right)}$$

# TTL Fan-Out



- Example

Calculate the maximum fan-out of TTL circuits assuming:

$V_{CE}(sat)=0.2V$, $V_{BE}(FA)=0.7V$, $V_{BE}(sat)=0.8V$, $V_{CC}=5V$, $R_B=4k\Omega$, $R_C=1.6k\Omega$, $R_{CP}=120\Omega$, $R_D=1k\Omega$, $\beta_F=25$, $\beta_R=0.1$, and $\sigma_{OL}=0.85$

- Solution

$$I_{IL}=\frac{5-0.8-0.2}{4}=1mA$$

$$I_{BS}(sat)=(1+1\times 0.1)\times\left(\frac{5-0.7-1.6}{4}\right)=0.743mA$$

$$I_{CS}(sat)=\frac{5-0.2-0.8}{1.6}=2.5mA$$

$$I_{ES}(sat)=0.743+2.5=3.243mA$$

$$I_{BO}=3.243-\frac{0.8}{1}=2.443mA$$

$$I_{OL}=0.85\times 25\times 2.443=51.9$$

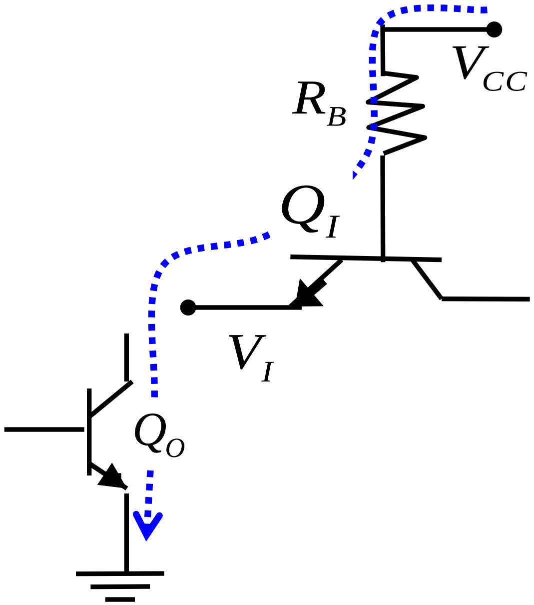
$$\boxed{M=51}$$

# TTL Power-Dissipation

Output high current supplied ($I_{CC}(H)$)
For High output,Input is low ($V_{CE}(sat)$)

$$\boxed{I_{CC}(OH) = I_{RB} = \frac{V_{CC} - V_{BE}(sat) - V_{CE,O}(sat)}{R_B}}$$

Since $Q_S$ is cut-off, and $I_{BP}$ is very small



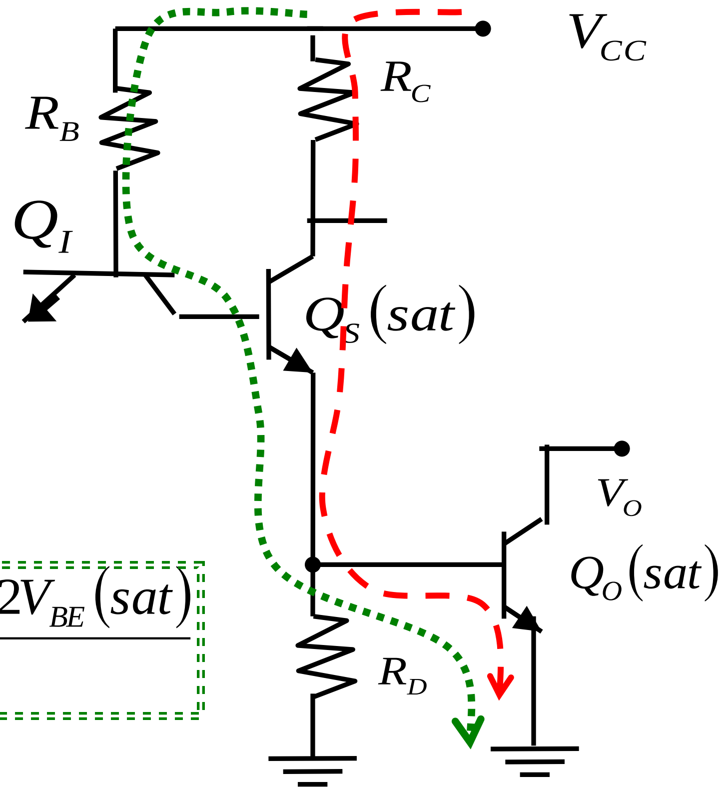
# TTL Power-Dissipation

Output low current supplied ($I_{CC}(L)$)
For Low output,Input is <u>High</u>

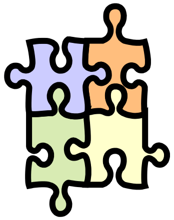
$$I_{CC}(OL) = I_{RC}(sat) + I_{RB}(RA)$$

$$I_{RC}(sat) = \frac{V_{CC} - V_{CE,S}(sat) - V_{BE,0}(sat)}{R_C}$$

$$I_{RB}(RA) = \frac{V_{CC} - V_{BC,I}(RA) - 2V_{BE}(sat)}{R_B}$$



# TTL Power-Dissipation



- Example

Calculate the average dissipated power of standard TTL circuits assuming:

$V_{CE}(sat)=0.2V$, $V_{BE}(FA)=0.7V$, $V_{BE}(sat)=0.8V$, $V_{CC}=5V$, $R_B=4k\Omega$, $R_C=1.6k\Omega$, $R_{CP}=100\Omega$, $R_D=1k\Omega$, and $\beta_F=100$.

- Solution

$$\boxed{I_{CC}(OH)=I_{RB}=\frac{5-0.8-0.2}{4}=1mA}$$

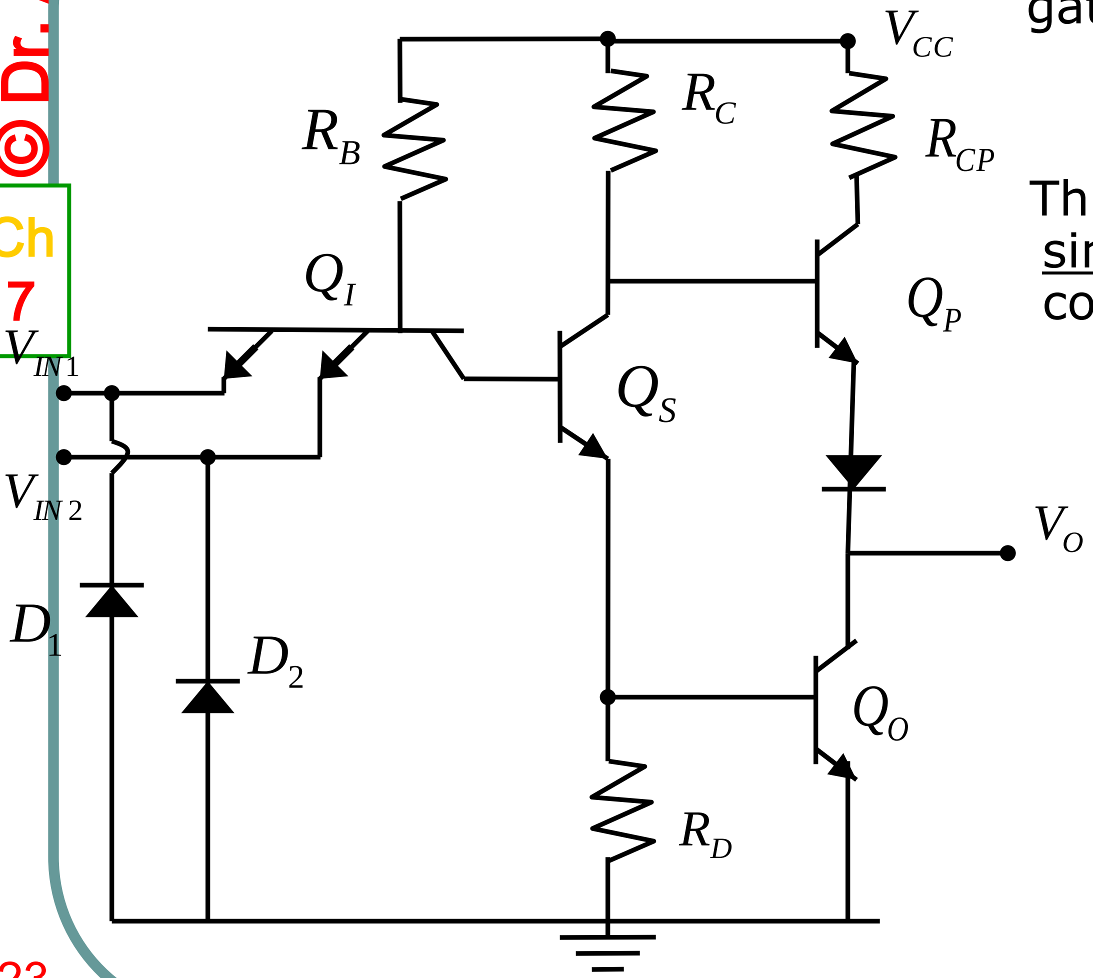
$$\boxed{\begin{aligned}I_{CC}(OL)&=\frac{5-0.2-0.8}{1.6}+\frac{5-0.7-1.6}{4}\\&=2.5+0.675=3.175mA\end{aligned}}$$

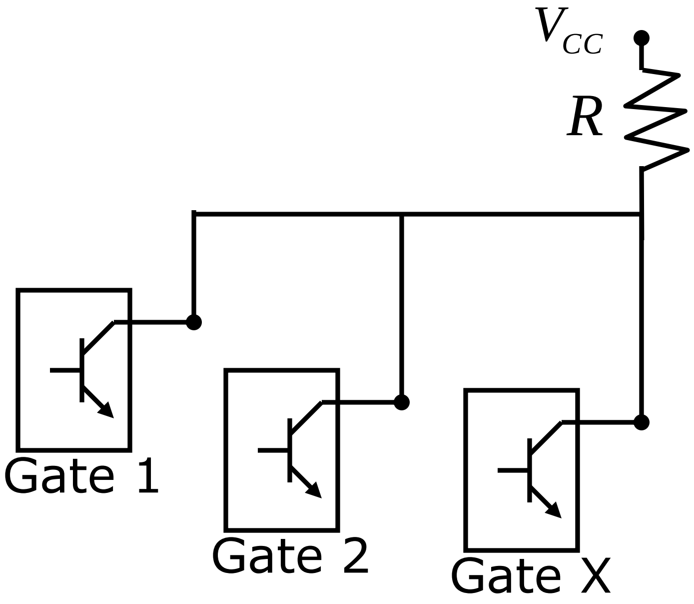
$$\boxed{P_{CC}(avg)=0.5\times4.175\times5=10.44mW}$$

# Open Collector TTL

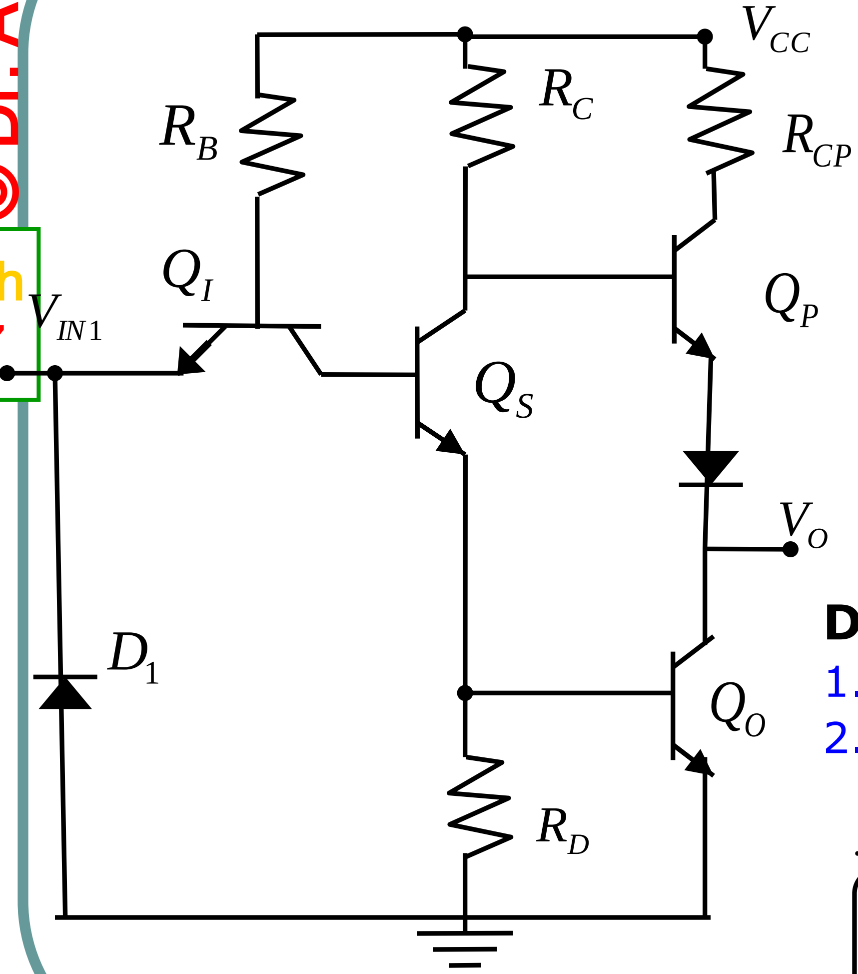
This is used when multiple output gates must be **ANDed**

This is accomplished by using single pull-resistor with open collector TTL gates ‘Wired-AND‘





# Low Power TTL (LTTL)



This is achieved by increasing resistor values by one order of magnitude

$R_B \uparrow$ $R_C \uparrow$

$I_{CC}(OL)$ & $I_{CC}(OH) \downarrow$

$I_{CC}(OL) \downarrow$

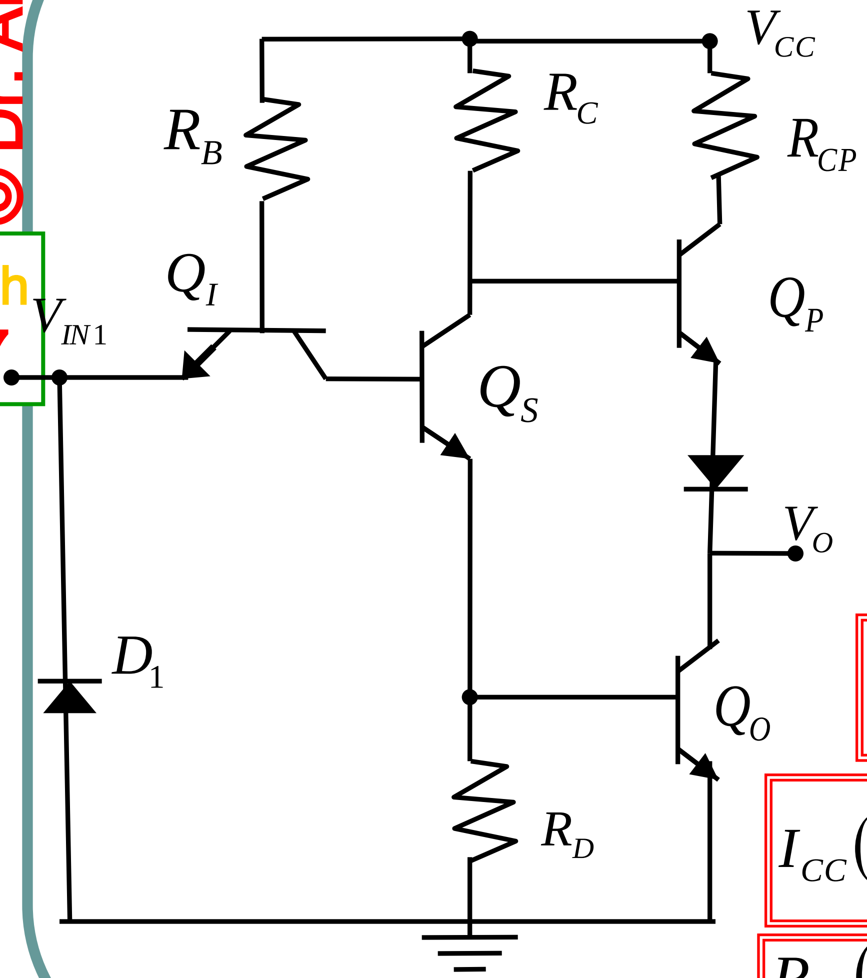
$\Rightarrow P_{CC}(avg) \downarrow$

**Disadvantages:**

1. Fan-Out decreases (*refer to slides 16 &17*)
2. Switching speed decreases (transient response gets longer)

Trade off exists between power dissipation and transient response

# Low Power TTL (LTTL)



- Previous example

$R_B$=4kΩ, $R_C$=1.6kΩ, $R_{CP}$=100Ω, $R_D$=1kΩ

$$P_{CC}(avg)=10.44mW$$

- Example

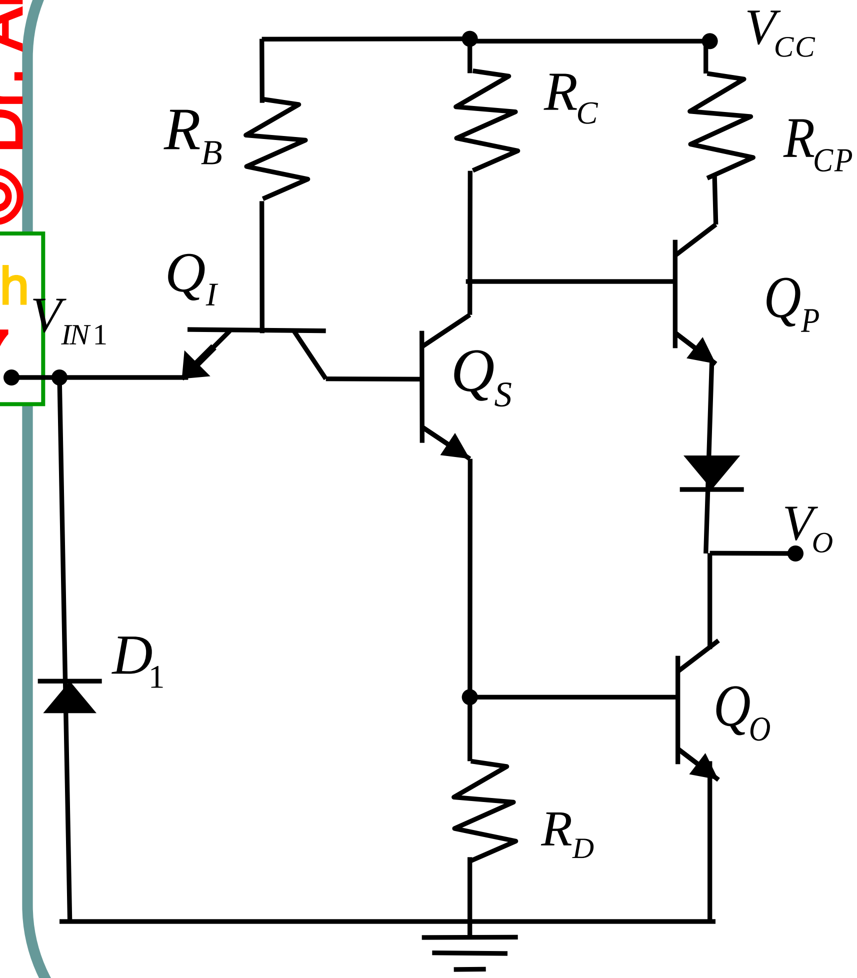
$R_B$=40kΩ, $R_C$=20 kΩ, $R_{CP}$=500Ω, $R_D$=12kΩ

$$I_{CC}(OH)=I_{RB}=\frac{5-0.8-0.2}{40}=0.1mA$$

$$I_{CC}(OL)=\frac{5-0.2-0.8}{20}+\frac{5-0.7-1.6}{40}=0.268mA$$

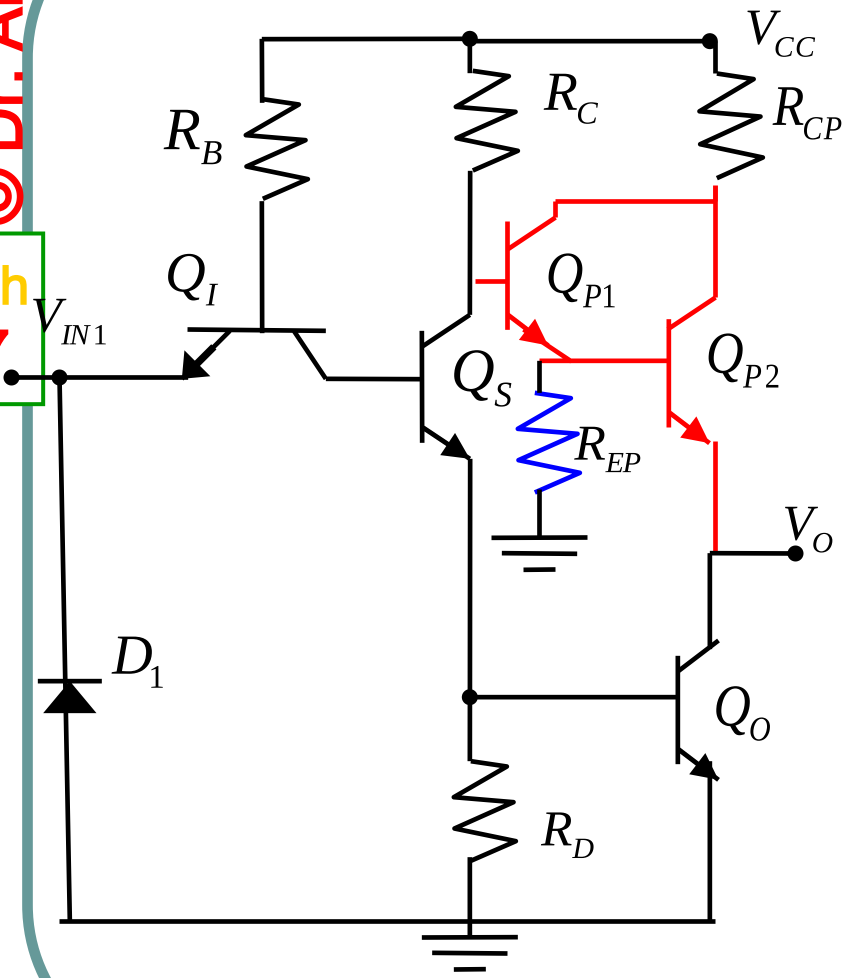
$$P_{CC}(avg)=0.5\times0.368\times5=0.919mW$$

# High Speed TTL (HTTL)



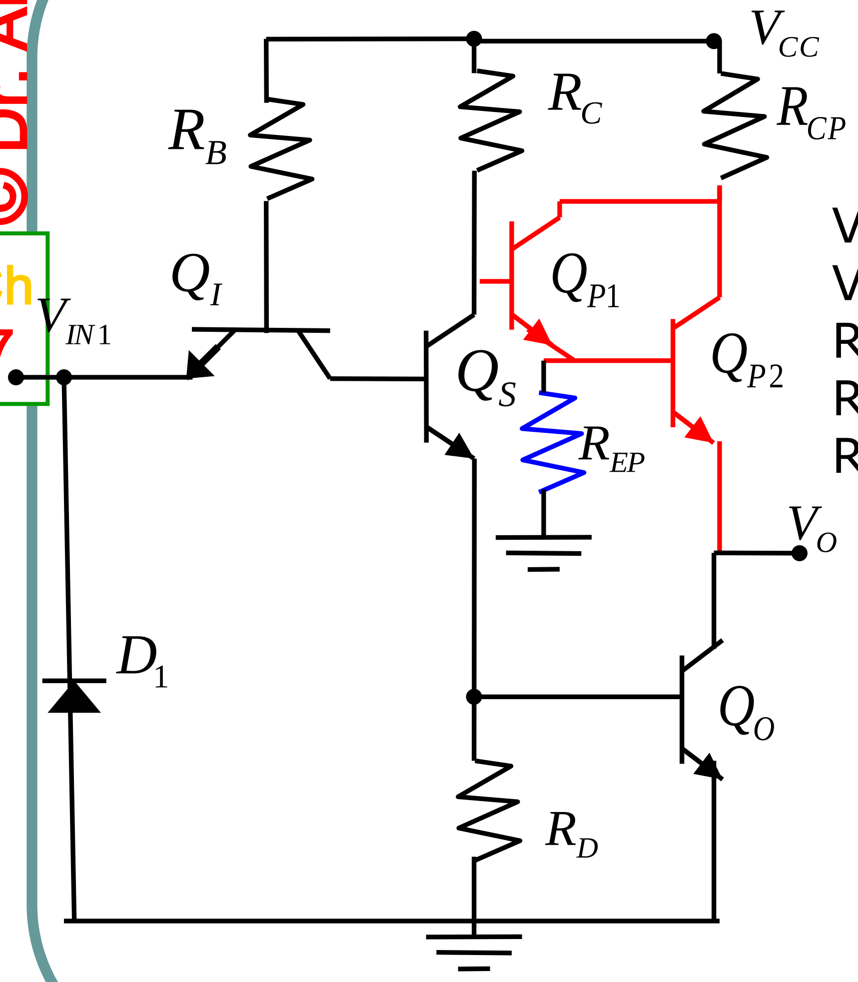
- Using smaller resistances increases the switching speeds

# High Speed TTL (HTTL)



- Using smaller resistances increases the switching speeds
- Using Darlington pair ($Q_{P1}$, $Q_{P2}$) instead of $Q_P$ increases the charging current of the load capacitance
- $R_{EP}$ is used as a discharge path for the base of $Q_{P2}$.

# High Speed TTL (HTTL)



- Example (Prob. 7.18

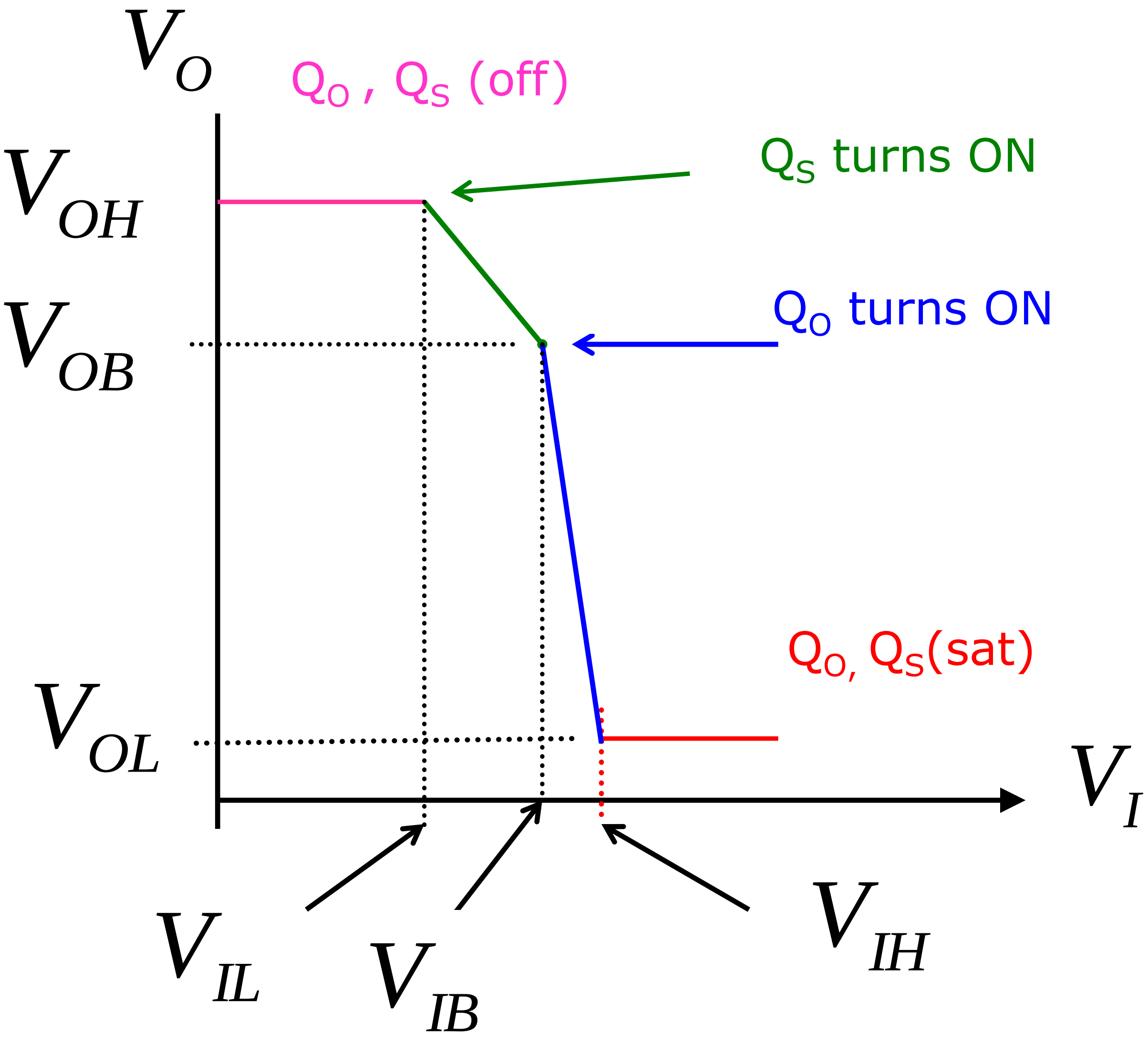
Plot the VTC of the HTTL circuits assuming:

$V_{CE}$(sat)=0.2V, $V_{BE}$(FA)= $V_{BC}$(RA)= 0.7V, $V_{BE}$(sat)=0.8V, $V_{CC}$=5V, $R_B$=2.8kΩ, $R_C$=760Ω, $R_{CP}$=58Ω, $R_{EP}$=4kΩ, $R_D$=470Ω, and $\beta_F$=70.

- Solution

*Refer to lecture class*

- HW #7:Solve Problems:7.1 , 7.5, 7.6, 7.9,7.11, and 7.12


$V_O$
$Q_O$ , $Q_S$ (off)
$V_{OH}$
$Q_S$ turns ON
$V_{OB}$
$Q_O$ turns ON
$Q_{O,}$ $Q_S$(sat)
$V_{OL}$
$V_I$
$V_{IL}$
$V_{IB}$
$V_{IH}$