Digital Electronics.

CHAPTER EIGHTTEEN

MOS Digital Integrated Circuits

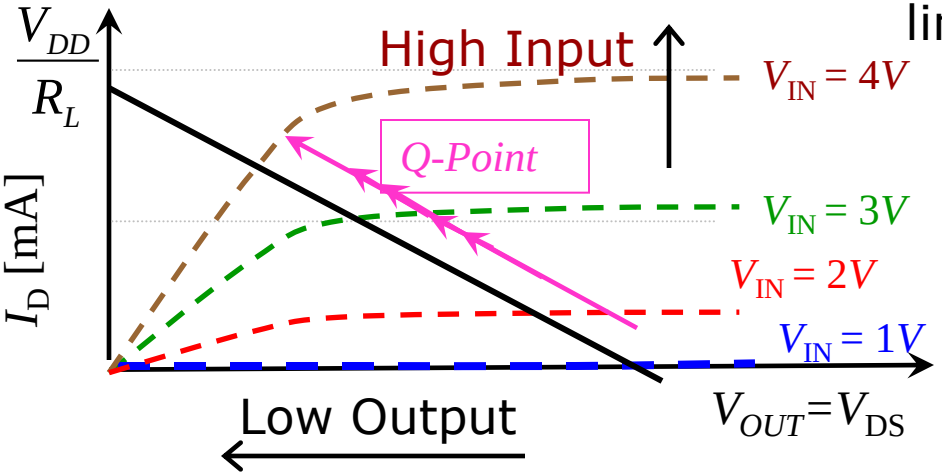
Power Dissipation of Resistor Loaded NMOS Inverter

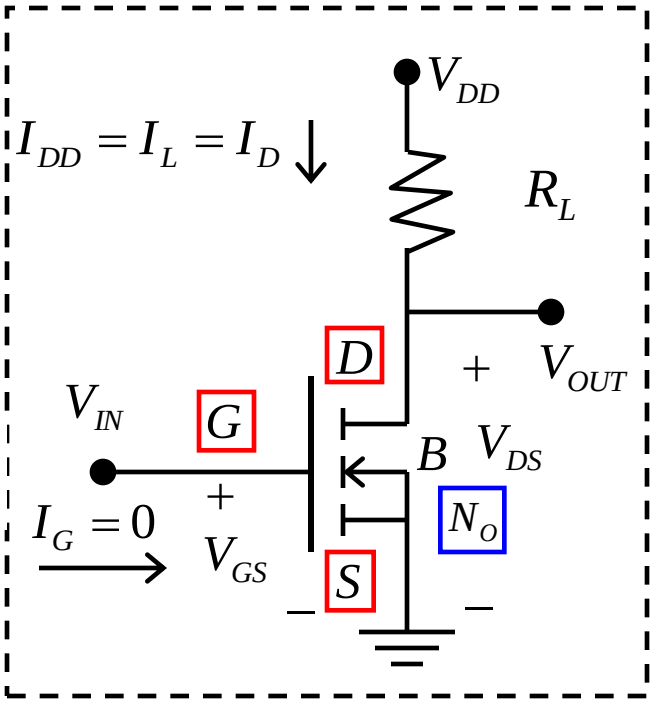
The currents supplied by V_{DD} for high and low states must be determined

Output high current supplied $I_{DD}(OH)$
For High output, Input is low ⇒ N_O is OFF

$$I_{DD}(OH) = 0$$

Output low current supplied $I_{DD}(OL)$
For Low output, Input is high ⇒ N_O operates in linear region





Power Dissipation of Resistor Loaded NMOS Inverter

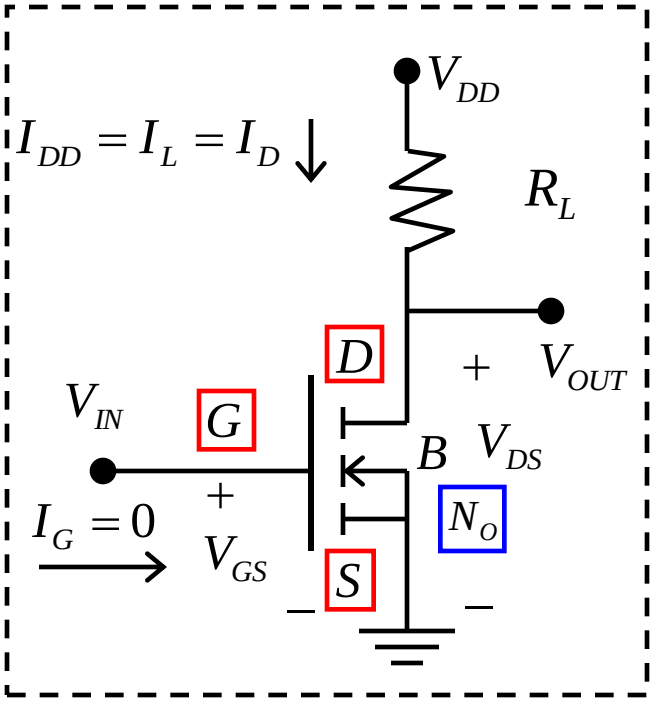
$I_{DD}(OL)$ ➡ N_O operates in linear region $\quad V_{GS} = V_{OH} = V_{DD} \quad V_{DS} = V_{OL}$

$$I_D = \frac{K_n}{2}\left[2\times(V_{DD} - V_{TN})V_{DS} - V_{DS}^2\right] = \frac{V_{DD} - V_{DS}}{R_L}$$

$$V_{DS} = V_{OL} \cong \frac{V_{DD}}{(V_{DD} - V_{TN})K_n R_L + 1} = V_{DS} \le (V_{GS} - V_{TN})$$

To ensure that N_O operates in linear mode

Slide 8 of last chapter



$$I_{DD}(OL) = \frac{K_n}{2}\left[2\times(V_{DD} - V_{TN})V_{OL} - V_{OL}^2\right]$$

Static Power Dissipation $\mathbf{P_{DD}(avg)}$

$$P_{DD}(avg) = V_{DD}\left(\frac{I_{DD}(OL) + I_{DD}(OH)}{2}\right) = V_{DD}\left(\frac{I_{DD}(OL)}{2}\right)$$

Power Dissipation of Resistor Loaded NMOS Inverter

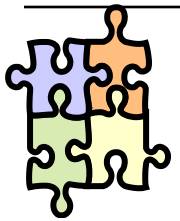
Dynamic Power Dissipation $P_{DD}(dyn)$

$$P_{DD}(dyn) = C_L \upsilon (V_{DD})^2$$

C_L is the total load capacitance at the output of the gate

υ is the switching frequency of the gate

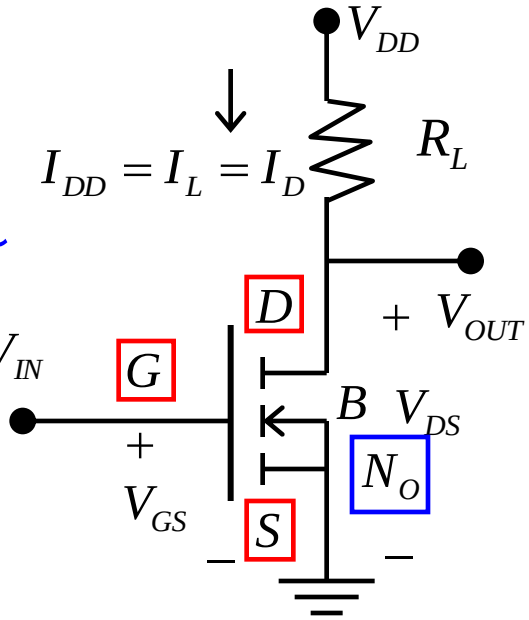
Power Dissipation of Resistor Loaded NMOS Inverter



Example

(a) Calculate the static dissipated power in the driver gate for the last example

V_{DD}=5V, V_T=1 V, k_n=40μA/V², R_L=50kΩ,



Slide 8 of last chapter

Solution (Exact Sol.)

$$V_{OL} = \left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right] \pm \sqrt{\left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right]^2 - \frac{2}{K_n}\frac{V_{DD}}{R_L}}$$

$V_{OL} = 4.5 \pm 3.905$ $\quad V_{OL} = 0.595V$ ✓ $\quad V_{OL} = 8.41V$ ✗

$V_{OL} = V_{DS} \le (V_{GS} - V_{TN})$ $\quad V_{OL} = V_{DS} \le (5-1)$

To ensure that N_O operates in linear mode

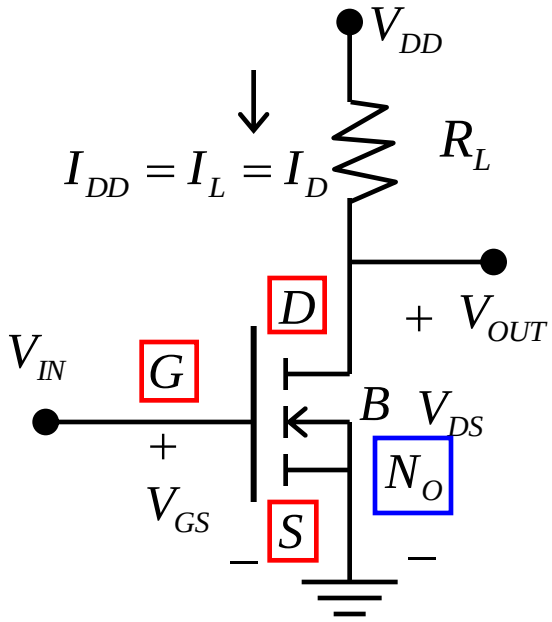
Power Dissipation of Resistor Loaded NMOS Inverter

Cont.

Example

(a) Calculate the static dissipated power in the driver gate for the last example

V_{DD}=5V, V_T=1 V, k_n=40μA/V², R_L=50kΩ,



Solution (Exact Sol.)

$$V_{OL} = 0.595V$$

$$I_{DD}(OL) = \frac{V_{DD} - V_{OL}}{R_L} = \frac{5 - 0.595}{50k} = 88.1\mu A$$

$$I_{DD}(OL) = \frac{K_n}{2}\left[2\times(V_{DD} - V_{TN})V_{DS} - V_{DS}^2\right] = 20\times10^{-6}\left(2\times4\times0.595 - 0.595^2\right) = 88.1\mu A$$

$$P_{DD}(avg) = 5\left(\frac{88.1}{2}\right) = 0.22mW$$

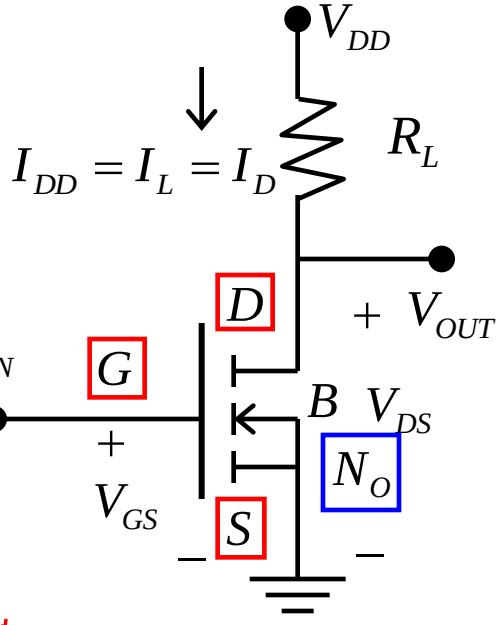
Power Dissipation of Resistor Loaded NMOS Inverter

Cont.

○ Example

(a) Calculate the static dissipated power in the driver gate for the last example

V_{DD}=5V, V_T=1 V, k_n=40μA/V², R_L=50kΩ,



○ Solution (Approx. Sol.)

$$V_{OL} \cong \frac{V_{DD}}{(V_{DD}-V_{TN})K_n R_L + 1} = \frac{5}{(5-1)\times 40\times 10^{-6}\times 50\times 10^{3}} = 0.556V$$

$$I_{DD}(OL) = \frac{V_{DD}-V_{OL}}{R_L} = \frac{5-0.556}{50k} = 88.89\mu A$$

Diff. due to approx.

$$I_{DD}(OL) = \frac{K_n}{2}\left[2\times(V_{DD}-V_{TN})V_{DS} - V_{DS}^2\right] = 20\times 10^{-6}\left(2\times 4\times 0.556 - 0.556^2\right) = 82.8\mu A$$

$$P_{DD}(avg) = 5\left(\frac{82.8}{2}\right) = 0.207mW$$

Power Dissipation of Resistor Loaded NMOS Inverter

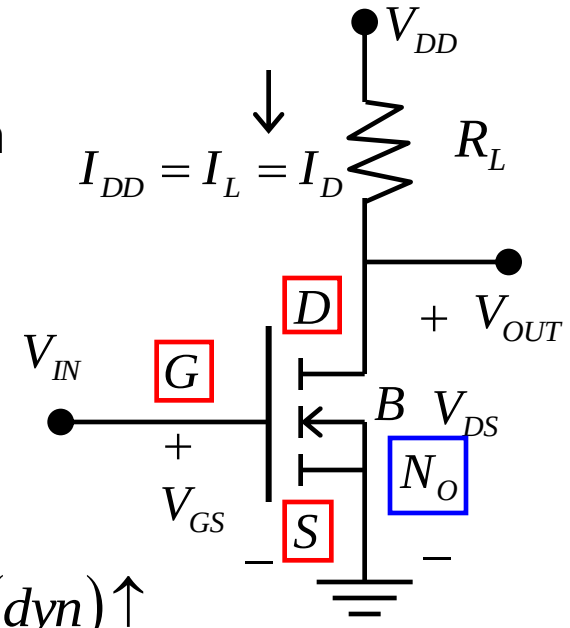
Cont.

Example

(b) Calculate the dynamic dissipated power in the driver gate for the last example

V_{DD}=5V, V_T=1 V, k_n=40μA/V², R_L=50kΩ,

C_L=1 pF, and $\upsilon = 1MHz$



Solution

$$P_{DD}(dyn) = C_L \upsilon (V_{DD})^2$$

$$P_{DD}(dyn) = 10^{-12} \times 10^6 \times 25 = 25\mu W$$

$$C_L \uparrow \Rightarrow P_{DD}(dyn) \uparrow$$

$$C_L = C'_{G1} + C'_{G2} + \cdots \quad \textit{parallel}$$

Note: In resistor loaded NMOS inverter, the dynamic dissipated power is less than the static dissipated power

- HW #10:Solve Problems: 18.**1-3**,