CHAPTER FIVE

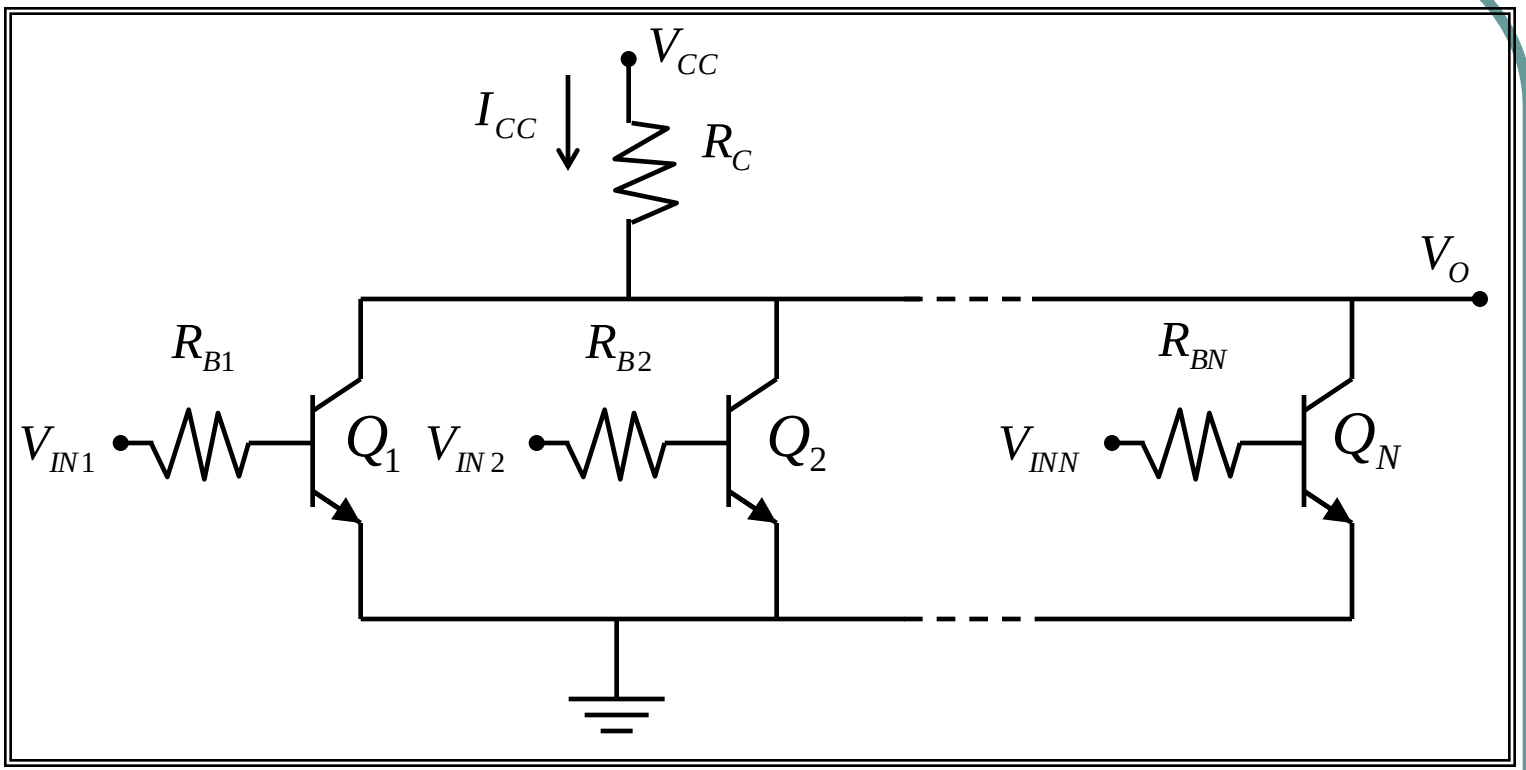
RTL NOR Gate

Digital Electronics.

Introduction

- RTL Inverter: discussed in Ch.4
- RTL NOR gate
- RTL NAND gate
- RTL OR gate
- RTL AND gate

Basic RTL NOR Gate



$$I_{CC} = \sum_{n=1}^{N} I_{Cn}$$

$$Vo = V_{CC} - I_{CC}R_C$$

If all inputs are less than V_{BE}(FA) ⇒ $V_O = V_{CC}$

If at least one input is greater than V_{IH} ⇒ $V_O = V_{CE}(sat)$

High

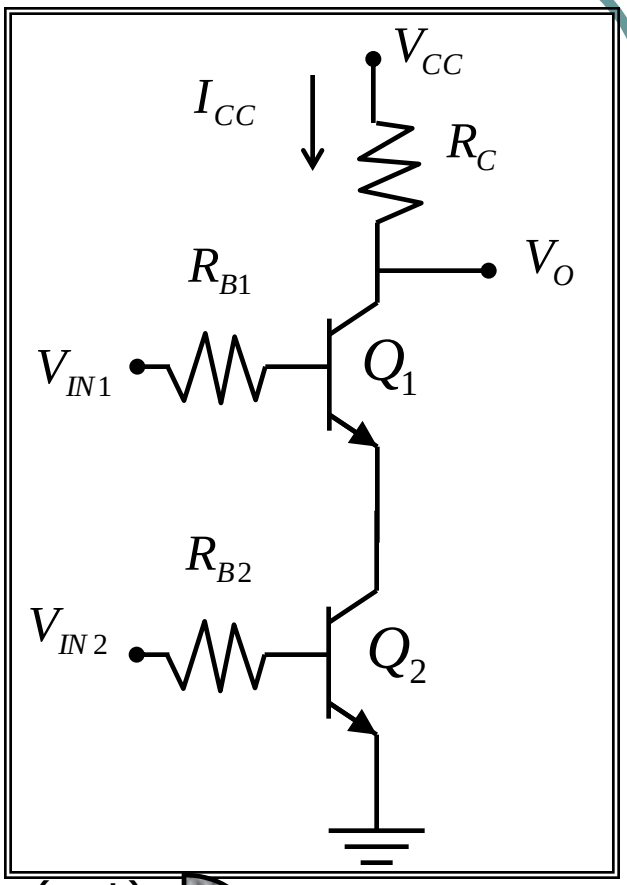
Low

Basic RTL NAND Gate

Assuming $\beta_F >> 1$, I_B is negligible to I_C

$$I_{CC} = I_{C1} \cong I_{E1} \cong I_{E2}$$

$$Vo = V_{CC} - I_{CC} R_C$$



If at <u>least one input</u> less than V_{BE}(FA), then the corresponding Q is off. i.e. $I_{CC}=0$

$$V_{OH} = V_{CC} \qquad V_O = V_{CE}(sat)$$

Q_2 starts conducting (ON) if $V_{IN2} > V_{BE2}$(FA)

Q_1 starts conducting (ON) if $V_{IN1} > V_{BE1}$(FA)+ V_{CE2}(sat)

V_O starts decreasing below V_{CC}

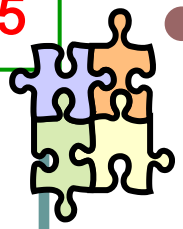
If both Q_1 and Q_2 are saturated
$V_O = 2V_{CE}$(sat)

Multi-Input RTL NAND Gate

$$V_{OH} = V_{CC} - I_{CC}R_C$$

$$V_{OL} = \sum_{n=1}^{N} V_{CEn}(sat)$$

Note: Number of inputs of an RTL NAND is limited



- **Example**

Determine the maximum fan-in for basic RTL NAND gate, assuming $V_{CE}(sat)=0.2V$, $V_{BE}(FA)=0.7V$

- **Solution**

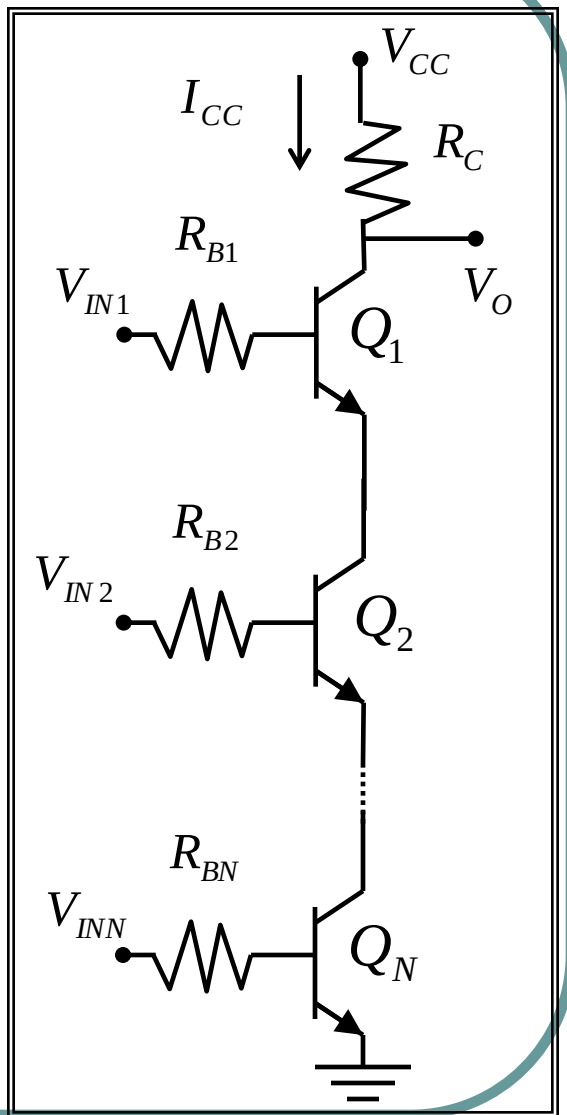
MUST $N_{ML} = V_{IL} - V_{OL} > 0 \qquad N_{MH} = V_{OH} - V_{IH} > 0$

$$V_{IL} > V_{OL} \Rightarrow 0.7 > N \times V_{CE}(sat)$$

$$N < \frac{0.7}{0.2} = 3.5 \Rightarrow N = 3$$

Always valid

$$V_{OH} > V_{IH} \Rightarrow V_{CC} > V_{BE}(FA) \surd$$



RTL Fan-Out

1. When an RTL gate is at output **low** state,then any load RTL gate will be in cut-off and draws **no** current

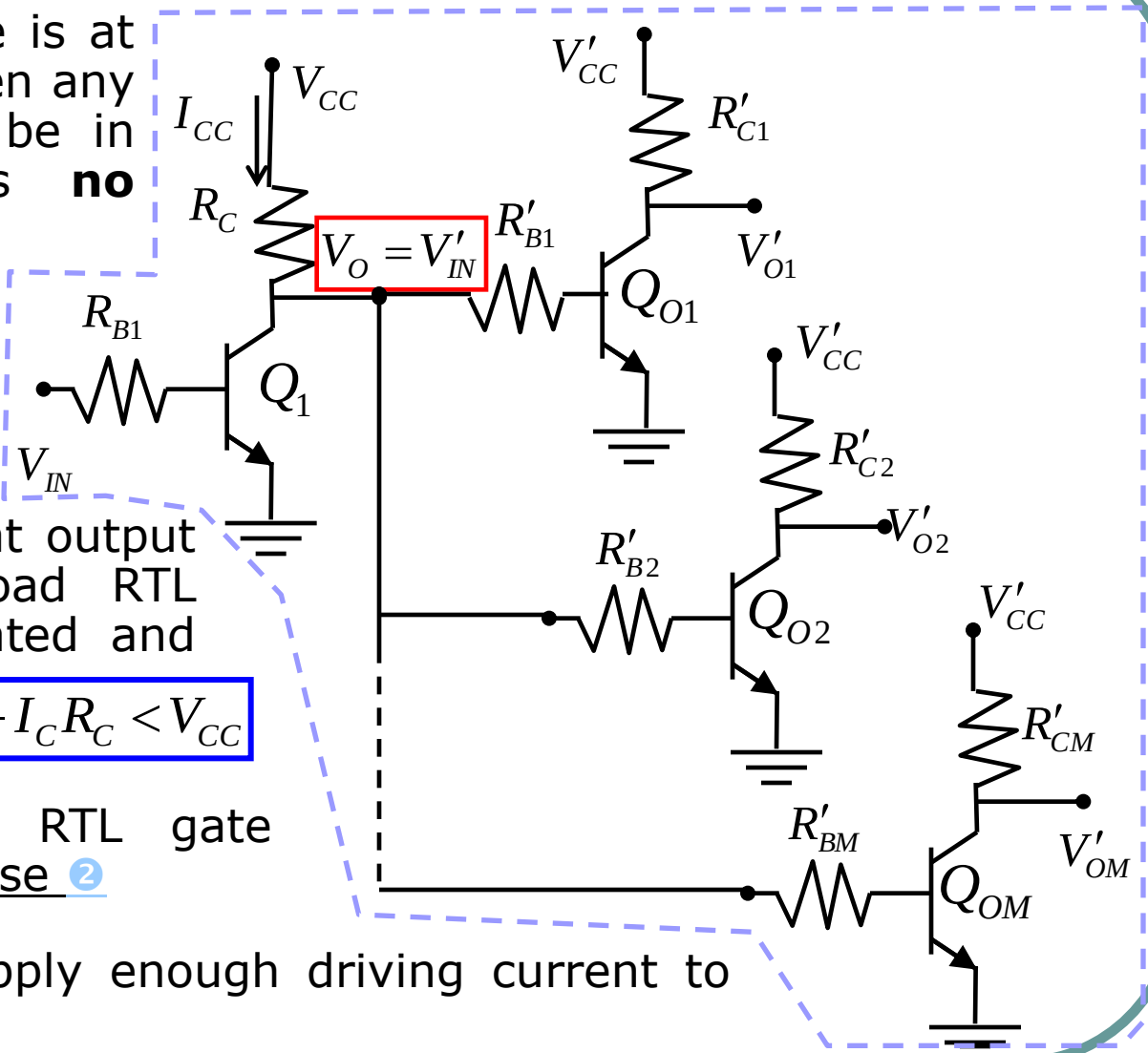
$$V_{OL} = V_{CE}(sat) = V'_{IN} < V_{BE}(FA)$$

2. When an RTL gate is at output **high** state,then all load RTL gates will be in saturated and draw current

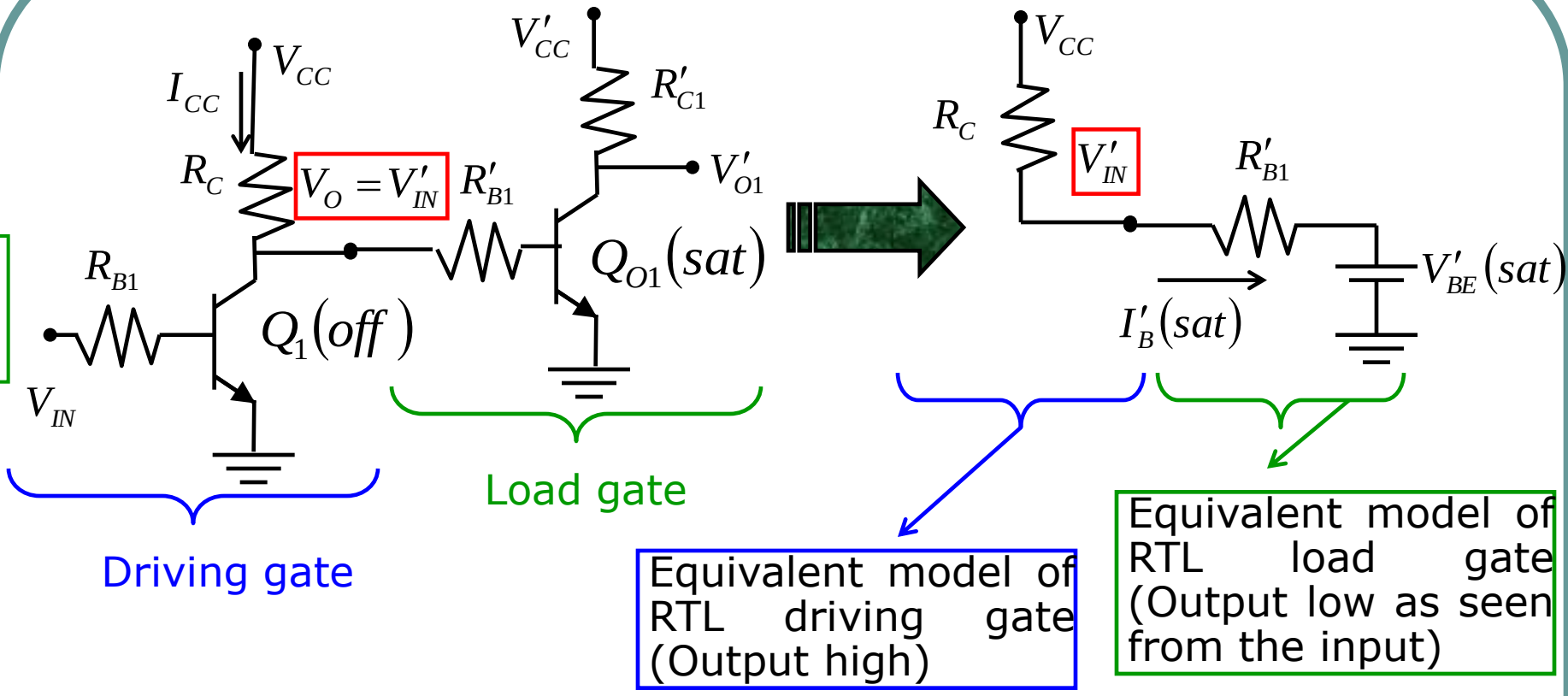
$$V_{OH} = V_{CC} - I_C R_C < V_{CC}$$

3. Maximum fan-out of RTL gate therefore depends on <u>case 2</u>

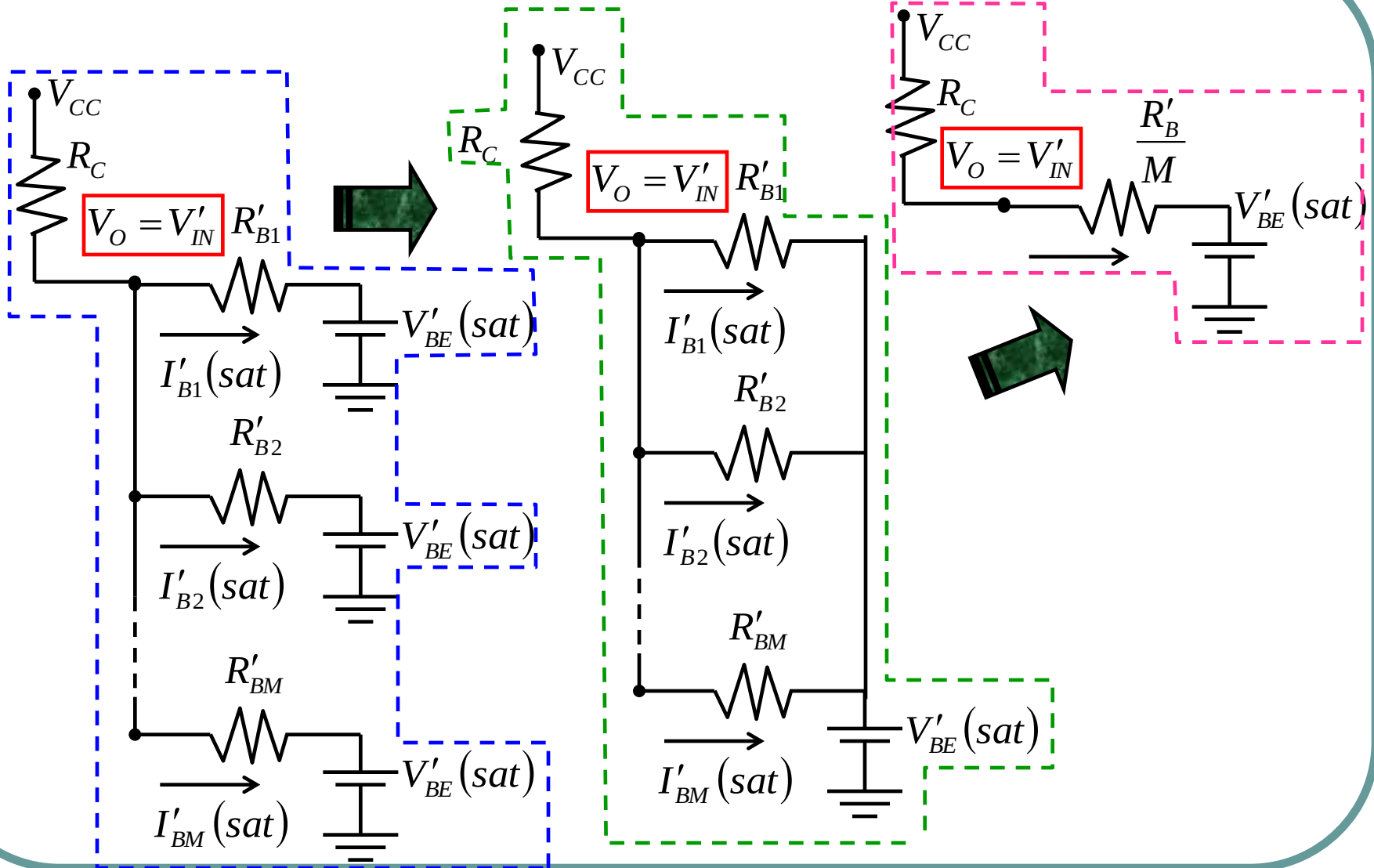
4. Driving gate must supply enough driving current to saturate all load gates



RTL Fan-Out



RTL Fan-Out

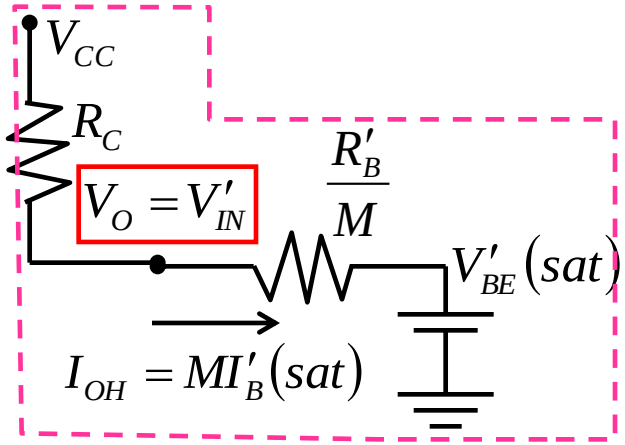


RTL Fan-Out

$$\frac{V_{CC}-V_O}{R_C}=\frac{V_O-V_{BE}(sat)}{R'_B/M}$$

$$M=\frac{(V_{CC}-V_O)/R_C}{(V_O-V_{BE}(sat))/R'_B} \quad \star$$

$$M=\frac{I_{OH}}{I_{IH}}$$



1. As M increases, the collector current of the driving gate increases, i.e. V_{OH} decreases. V_{OH} should be large enough to saturate all load gates

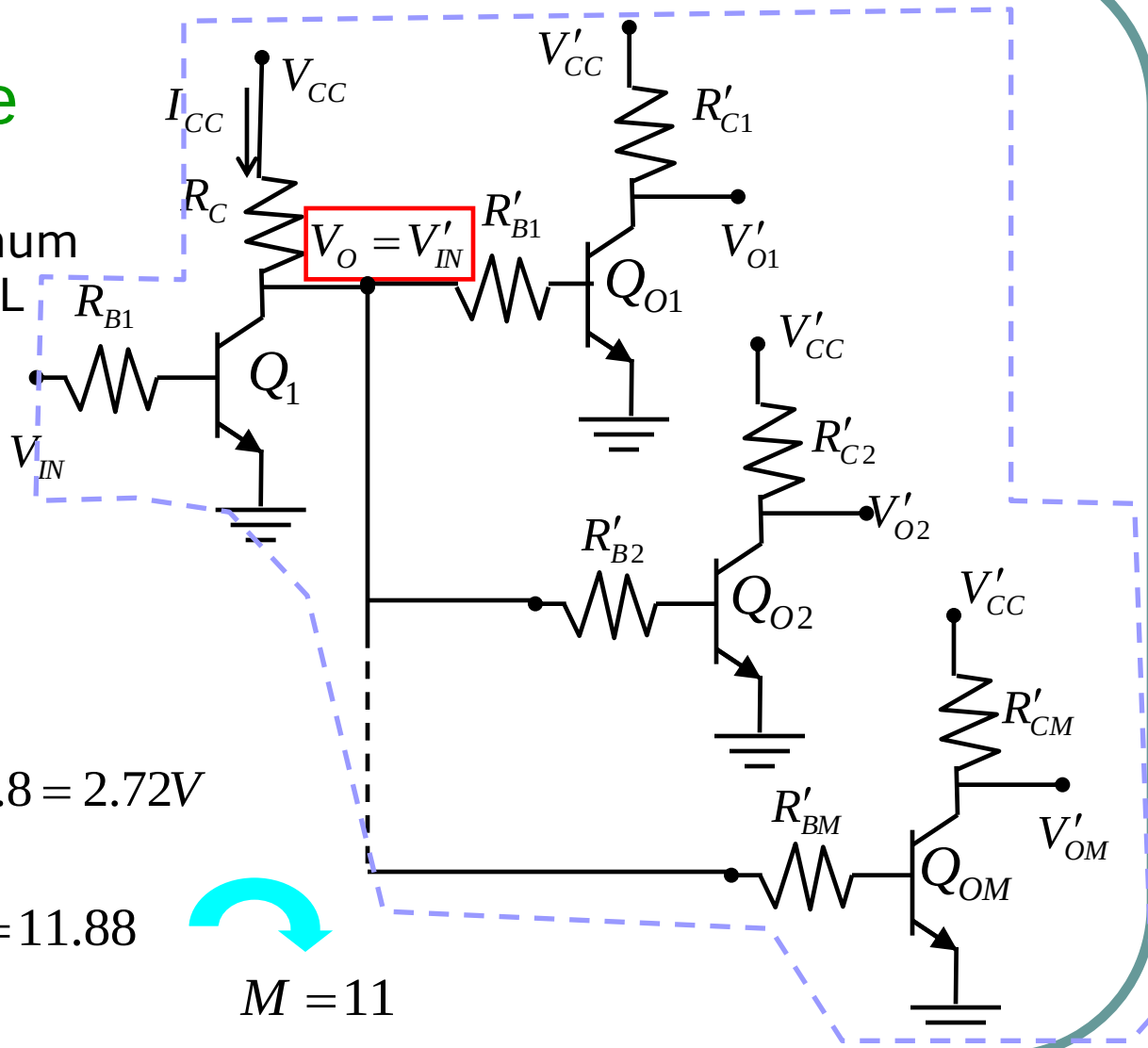
$$V_{OH}(\min)=V_{IH}=\frac{V_{CC}-V_{CE}(sat)}{\beta_F R'_C}R'_B+V'_{BE}(sat) \quad \star\star$$ (Proved in p. 10 of CH.4)

2. Now, substitutiong V_{OH}(min) ($\star\star$) as V_o in ($\star$) gives the maximum fan-out

RTL Fan-Out

Example

Determine the maximum fan-out for driving RTL gate, assuming $V_{CE}(sat)=0.2V$, $V_{BE}(sat)=0.8V$, $\beta_F=25, V_{CC}=5V$, $R_C=1k\Omega$, $R_B=10k\Omega$



Solution

$$V_{OH}(\min) = \frac{5-0.2}{25} \times 10 + 0.8 = 2.72V$$

But

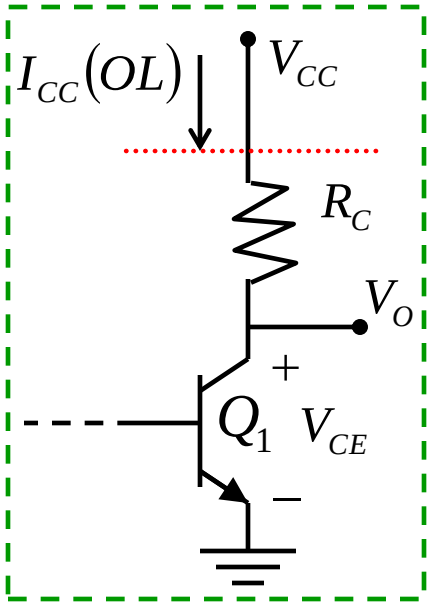
$$M = \frac{(5-2.72)/1}{(2.72-0.8)/10} = 11.88$$

$$M = 11$$

RTL Power-Dissipation

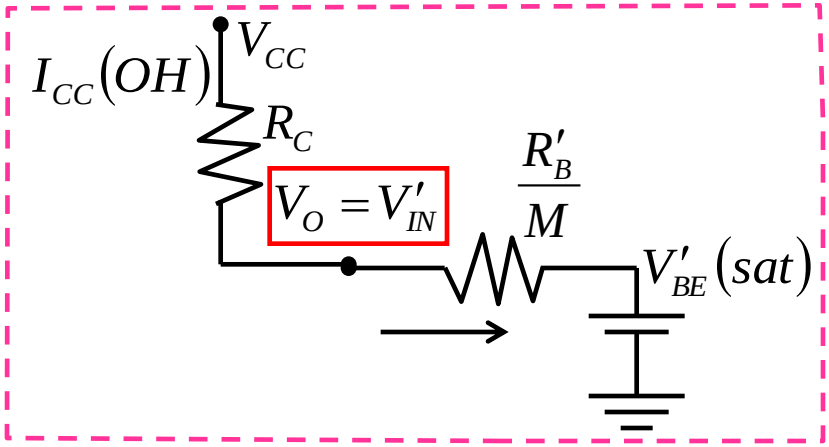
Output low supplied current = $I_{CC}(OL)$

$$I_{CC}(OL) = \frac{V_{CC} - V_{CE}(sat)}{R_C}$$



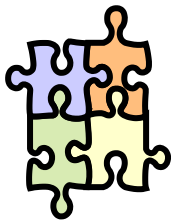
Output high supplied current assuming M-load gates = $I_{CC}(OH)$

$$I_{CC}(OH) = \frac{V_{CC} - V_{BE}(sat)}{R_C + \frac{R'_B}{M}}$$



$$P_{CC}(avg) = V_{CC}\left(\frac{I_{CC}(OH) + I_{CC}(OL)}{2}\right)$$

RTL Power-Dissipation



- **Example**

Determine the average dissipated power for
A. No load
B. Fan-out of 1
Assuming $V_{CE}(sat)=0.2V$, $V_{BE}(sat)=0.8V$, $\beta_F=25$, $V_{CC}=5V$, $R_C=1k\Omega$, $R_B=10k\Omega$

- **Solution**

A. No load:

$$I_{CC}(OL)=\frac{V_{CC}-V_{CE}(sat)}{R_C}=\frac{5-0.2}{1}=4.8mA$$

$$I_{CC}(OH)=0mA$$

$$P_{CC}(avg)=5\left(\frac{4.8}{2}\right)=12mW$$

B. *M*=1:

$$I_{CC}(OL)=\frac{V_{CC}-V_{CE}(sat)}{R_C}=\frac{5-0.2}{1}=4.8mA$$

$$I_{CC}(OH)=\frac{V_{CC}-V_{BE}(sat)}{R_C+\frac{R'_B}{M}}=\frac{5-0.8}{1+10}=0.382mA$$

$$P_{CC}(avg)=5\left(\frac{4.8+0.382}{2}\right)=12.96mW$$

Basic RTL Non-Inverter *(Emitter Follower in Analog Ccts)*

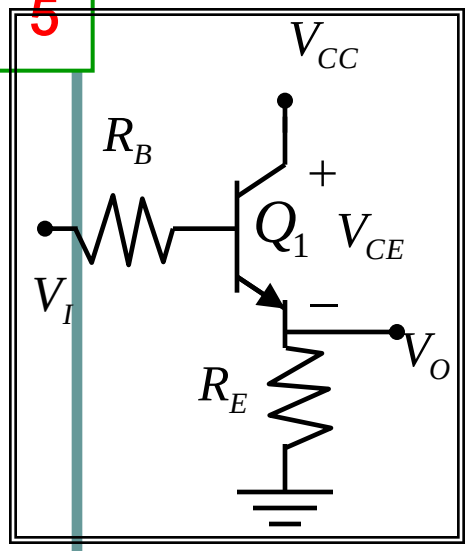
Ch 5

- Voltage-Transfer Characteristics

For $V_I - GND < V_{BE}(FA)$ ⇒ $I_B=0, I_C=0, V_O=0=V_{OL}$

For $V_I - GND \geq V_{BE}(FA)$ ⇒ $I_B=(V_I-V_{BE}(FA))/(R_B+(1+\beta_F)R_E)$, $V_O=R_E(V_I-V_{BE}(FA))/(R_B/(1+\beta_F)+R_E)$

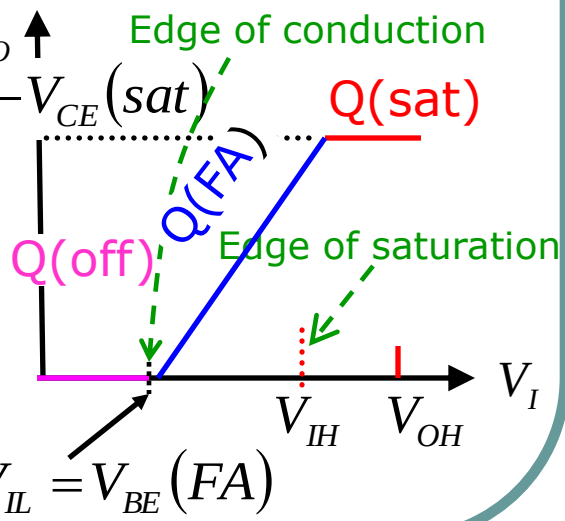
For $V_I - GND \geq V_{IH}$ ⇒ $I_E=(V_{CC}-V_{CE}(sat))/R_E$, $V_O=V_{CC}-V_{CE}(sat)=V_{OH}$



$$V_{IH} = I_B(sat)R_B + V_{BE}(sat) + I_E(sat)R_E$$

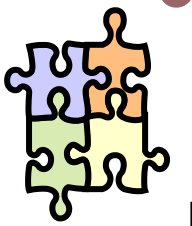
$$= I_E(EOS)\left(R_E + \frac{R_B}{(1+\beta_F)}\right) + V_{BE}(sat)$$

$$V_{OH} = V_{CC} - V_{CE}(sat)$$



$$V_{IH} = \frac{V_{CC} - V_{CE}(sat)}{R_E}\left(R_E + \frac{R_B}{(1+\beta_F)}\right) + V_{BE}(sat)$$

BJT Non-Inverter (Basic RTL Non-Inverter)



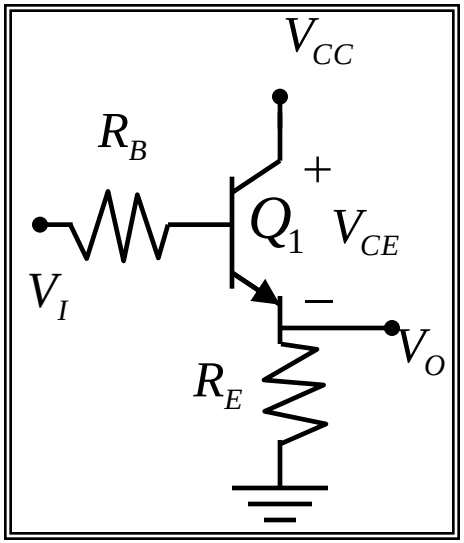
- Example

Assume V_{CC}= 5 V, R_E= 1kΩ , R_B= 10 kΩ, β_F=25;
V_{CE}(sat)=0.2V, V_{BE}(sat)=0.8V, V_{BE}(FA)=0.7V,

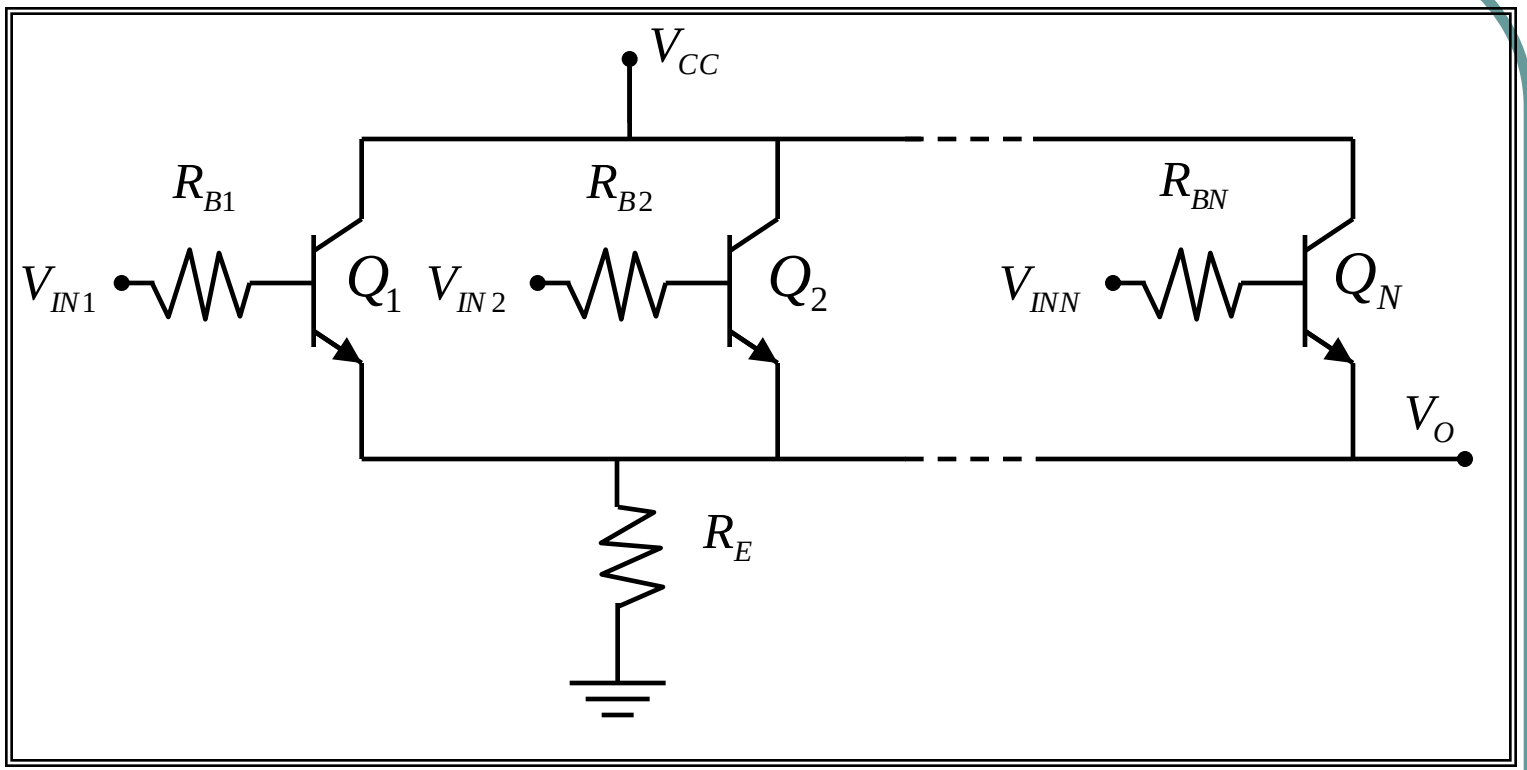
Determine the <u>VTC</u> parameters

- Solution

V_{IL}= 0.7 V, V_{IH}= 7.45 V,
V_{OL}= 0.0 V, V_{OH}= 4.8 V,



Basic RTL OR Gate



If all inputs are less than V_{BE}(FA) ⇒ $V_O = 0$ Low

If at least one input is greater than V_{IH} ⇒ $V_O = V_{CC} - V_{CE}(sat)$ High

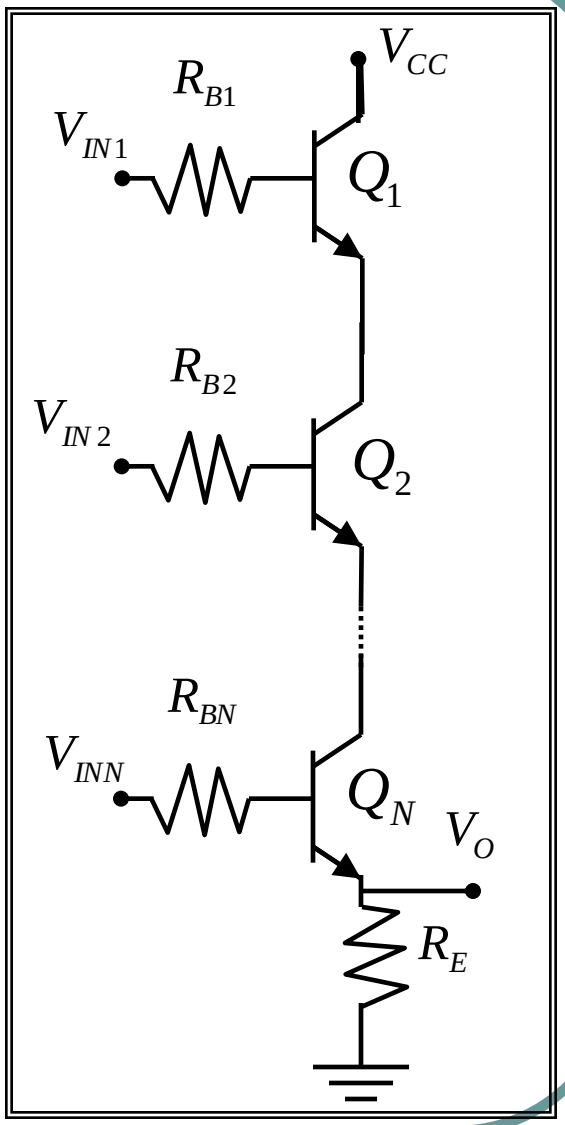
Basic RTL AND Gate

If at <u>least one input</u> less than V_{BE}(FA), then the corresponding Q is off. i.e. $I_E=0$

$$V_{OL} = 0$$

If <u>ALL inputs</u> are greater than V_{IH}, then the corresponding Q is saturated.

$$V_{OH} = V_{CC} - N \times V_{CE}(sat)$$



RTL With Active Pull-Up Inverter

The object is to incresae the fan-out of RTL inverter gate (gives more current).

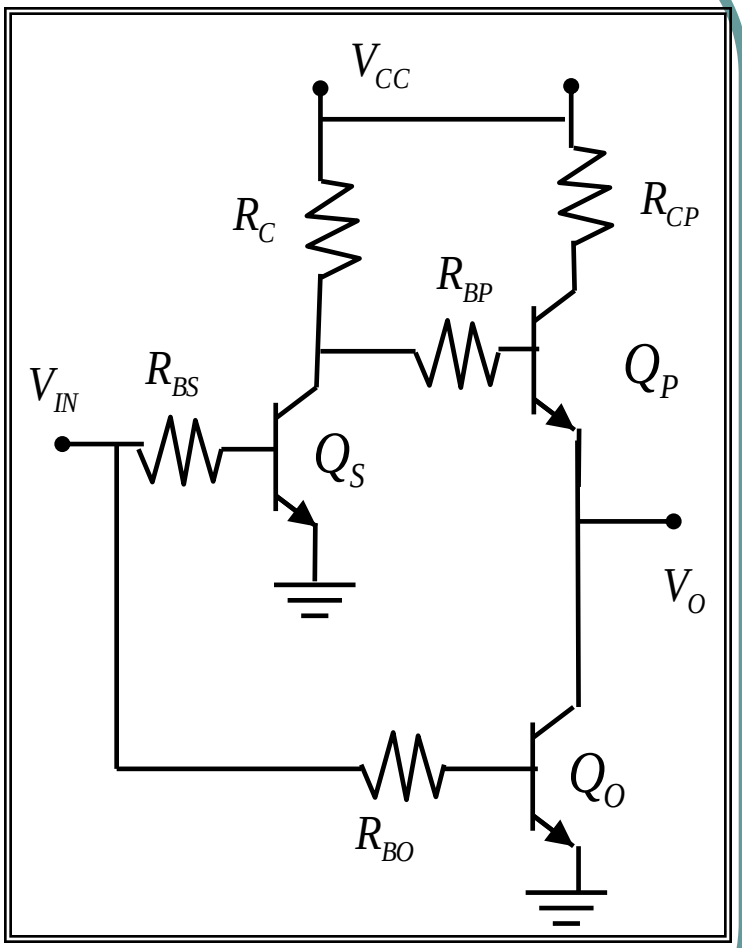
To accumplish active pull-up:

Basic assumptions: * $R_{CP} << R_C$

$R_{CP} \cong 0.1 \times R_C$

* $R_{BS} = R_{BO}$ and Q_O & Q_S turn ON and OFF simultaneously

* Q_S provides logic inversion for Q_P such that Q_S & Q_P never turn ON simultaneously



RTL With Active Pull-Up Inverter

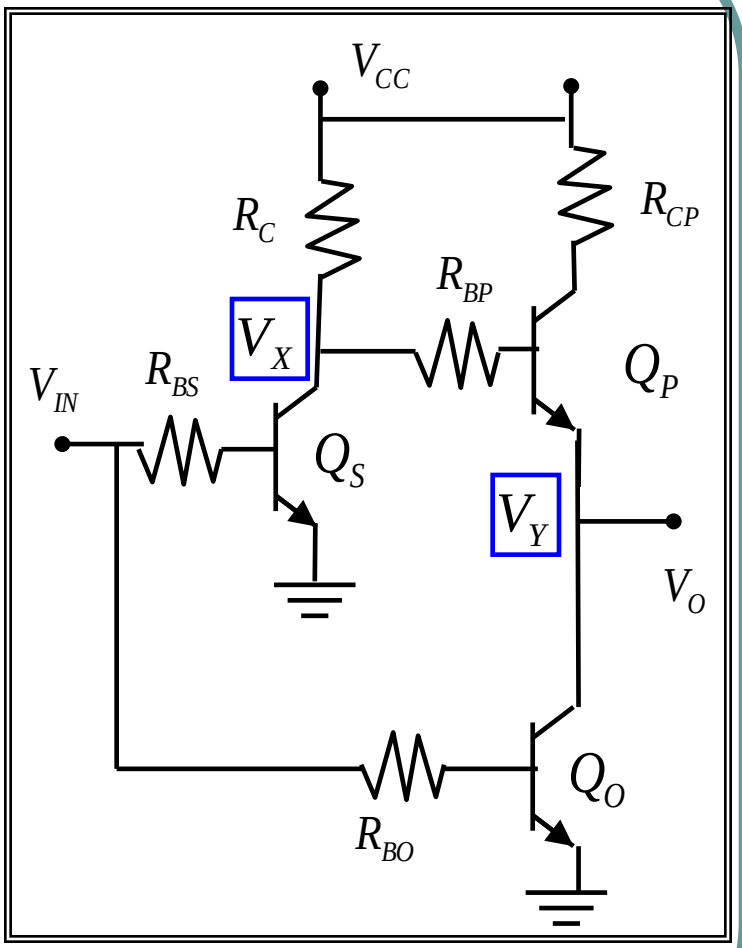
For $V_{IN} \geq V_{INH}$ (Logic High)

Q_O & Q_S are ON (sat) $V_X = V_Y = 0.2V$. → $V_X - V_Y < V_{BEP}$(FA). i.e. Q_P is cut-off (very very large resistance)

For $V_{IN} \leq V_{INL}$ (Logic Low)

Q_O & Q_S are cut-off
Q_P is ON (sat)

$$V_O = V_{CC} - V_{CE}(sat) - I_{CP}R_{CP}$$

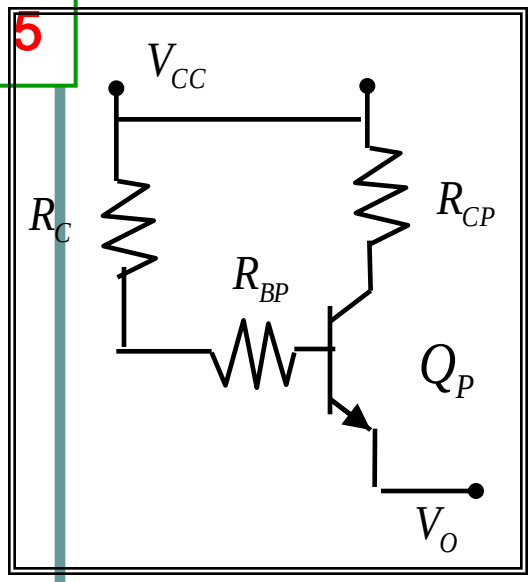


Fan-Out of RTL With Active Pull-Up Inverter

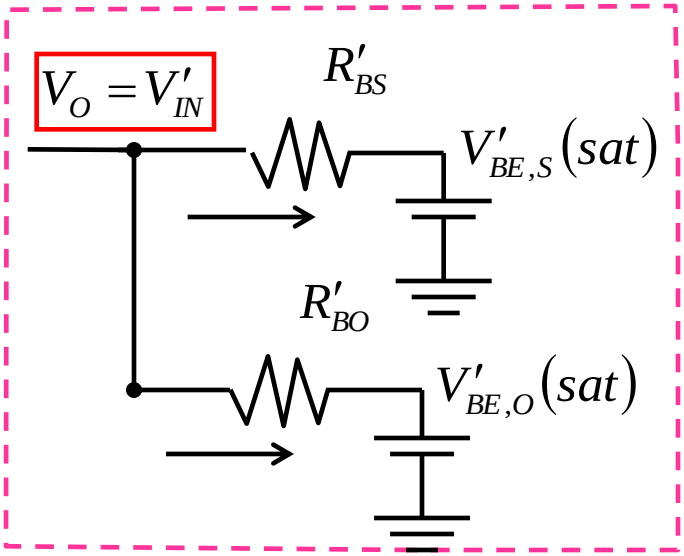
Fan-out is limited by the output high state of the driving gate

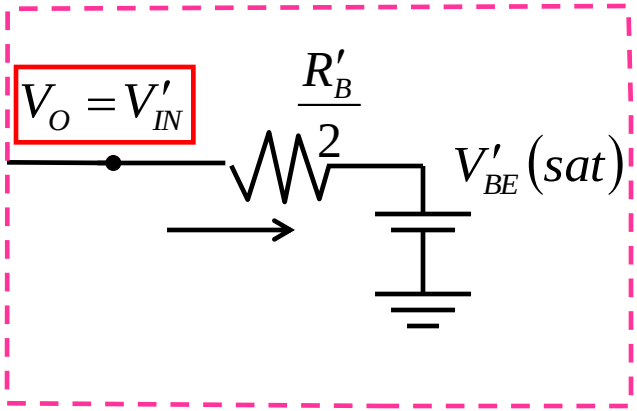
Q_O & Q_S are cut-off

Q_P is ON (sat)



Equivalent cct of driving gate when output is high





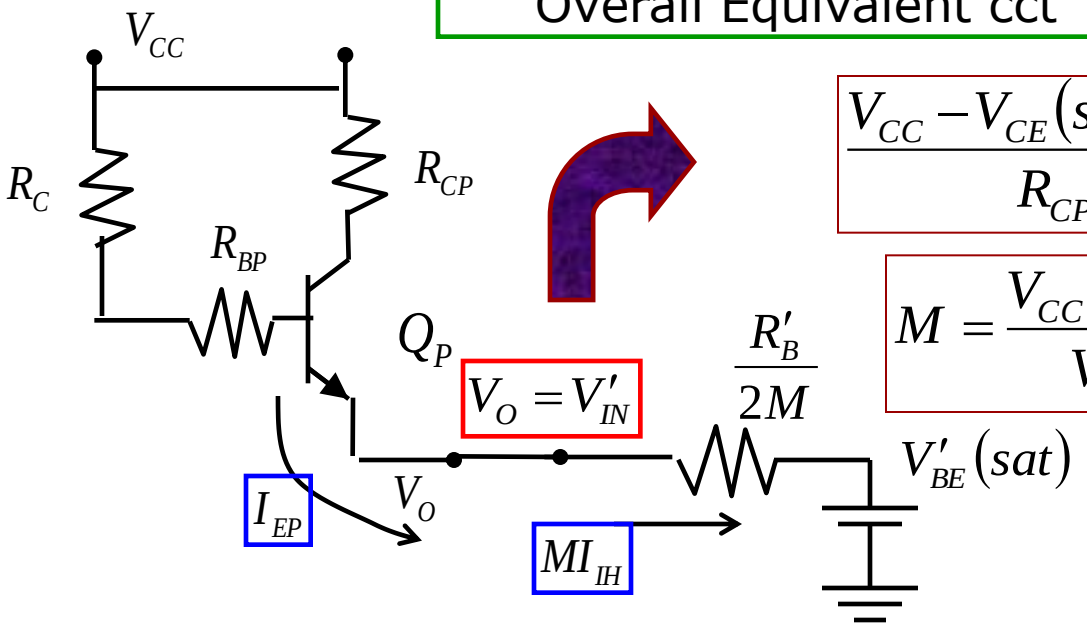
Equivalent cct of one load gate when input is high

Fan-Out of RTL With Active Pull-Up Inverter

Fan-out is limited by the output high state of the driving gate

Q_O & Q_S are cut-off
Q_P is ON (sat)

Overall Equivalent cct



$$\frac{V_{CC} - V_{CE}(sat) - V_O}{R_{CP}} = \frac{V_O - V_{BE}(sat)}{R'_B / 2M}$$

$$M = \frac{V_{CC} - V_{CE}(sat) - V_O}{V_O - V_{BE}(sat)} \times \frac{R'_B}{2R_{CP}}$$

As *M* increases, I_{EP} increases, then V_O decreases

Fan-Out of RTL With Active Pull-Up Inverter

The limiting factor for V_O is that it must be sufficient to saturate Q_S` and $Q_O$` of the load gates.

It is easy to saturate Q_S since its effective load seen by the collector is very large with negligible I_B since Q_P is cut-off

i.e. to saturate Q_S , we need:

$$V_{OH}(\min) = V_{IH} = V_{BE}(sat) + \frac{R_B}{\beta_F}\left(\frac{V_{CC} - V_{CE,S}(sat)}{R_C}\right)$$

(Proved also in p. 10 of CH.4)

Substitute in

$$M = \frac{V_{CC} - V_{CE}(sat) - V_O}{V_O - V_{BE}(sat)} \times \frac{R'_B}{2R_{CP}}$$

Fan-Out of RTL With Active Pull-Up Inverter

- Example

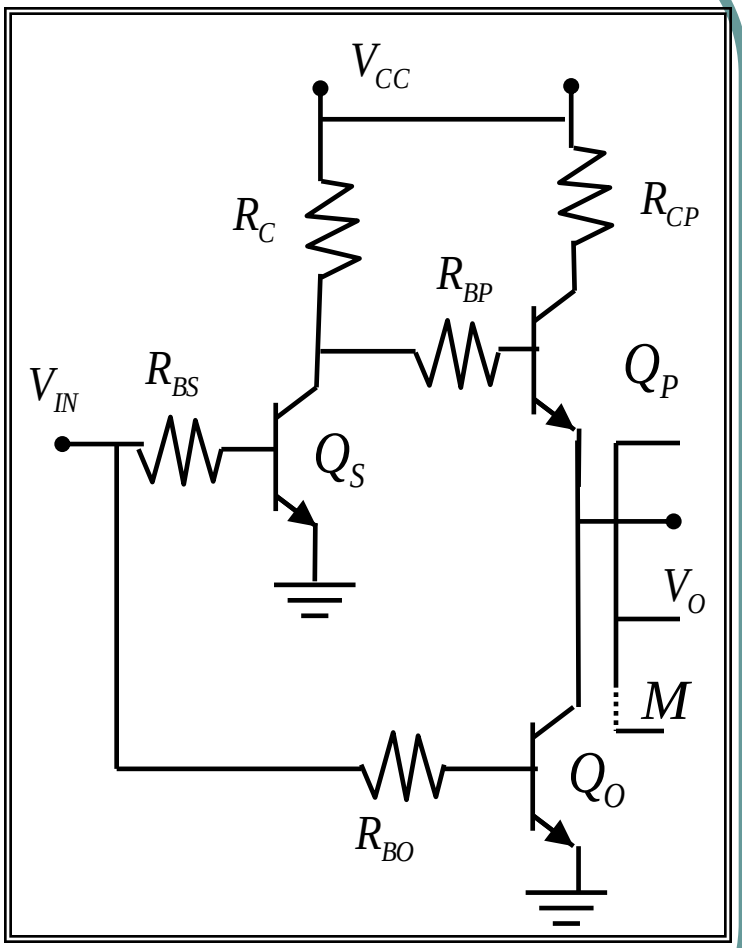
Determine the maximum fan-out for driving RTL gate, assuming $V_{CE}(sat)=0.2V$, $V_{BE}(sat)=0.8V$, $\beta_F=25$, $V_{CC}=5V$, $R_C=1k\Omega$, $R_{BO}=R_{BS}=10k\Omega$, $R_{CP}=100\Omega$.

- Solution

$$V_{OH}(\min)=0.8+\frac{10}{25}\left(\frac{5-0.2}{1}\right)=2.7V$$

$$M=\frac{5-0.2-2.7}{2.7-0.8}\times\frac{10}{2\times0.1}=55.3$$

$$M=55$$

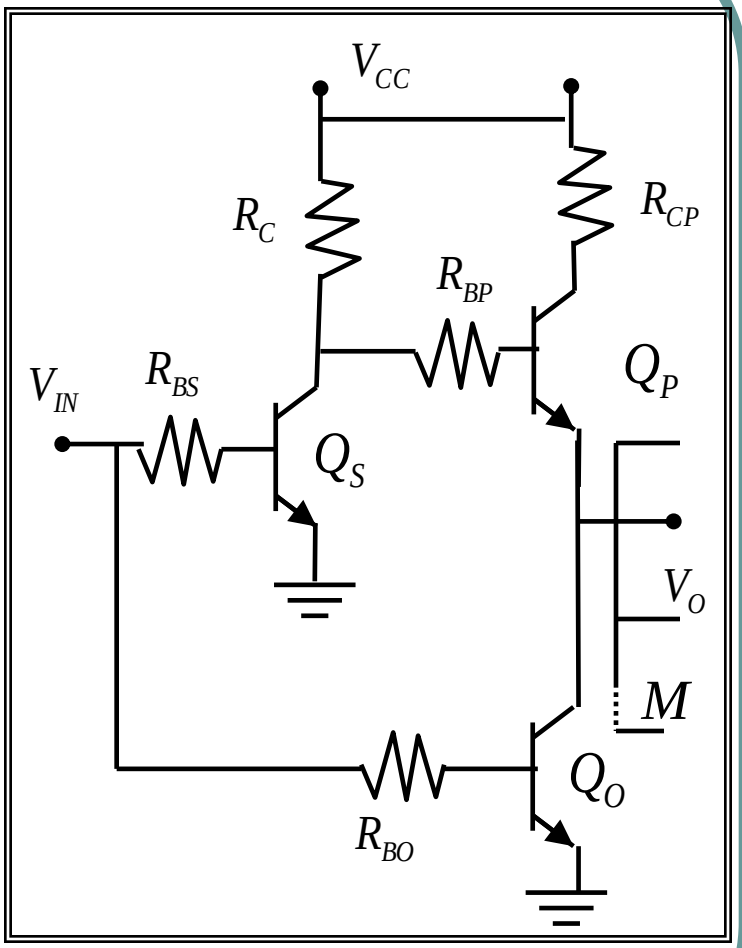


(without pull-up, *M* was 11. i.e. It increases 500%. See p. 10)

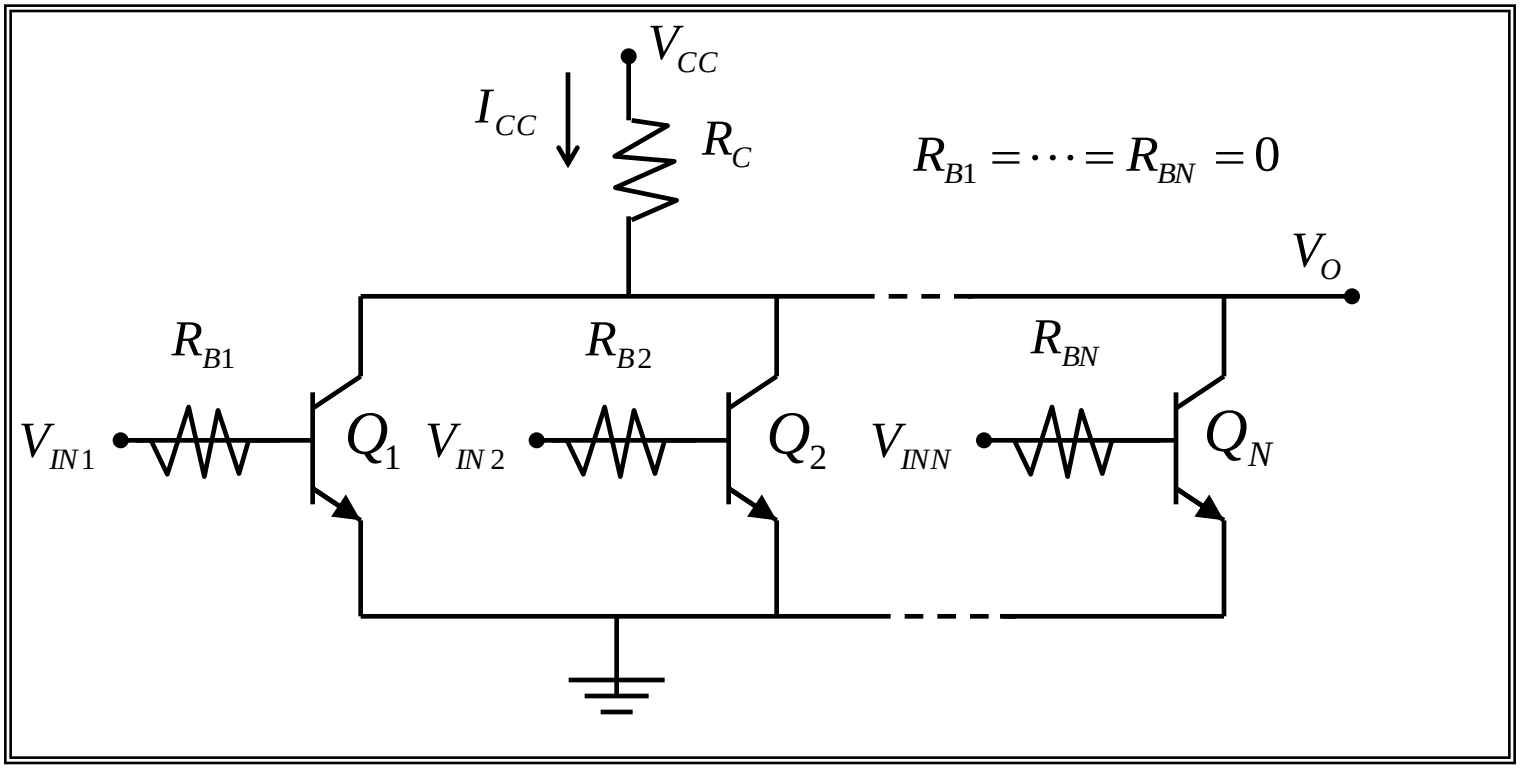
RTL SPICE Simulation

- Example

*Repeat the last example using PSPICE
*Plot V_O as a function of V_{IN}
*Refer to pages 67-68 in the text book.



Direct Coupled Transistor Logic

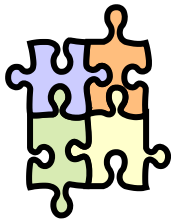


Three-input DCTL NOR gate

Advantage: Reduce the packing density of RTL in integrated circuits form since the base resistors are eliminated

Disadvantage: Current hogging when V_O is at logic high for fan-out greater than one

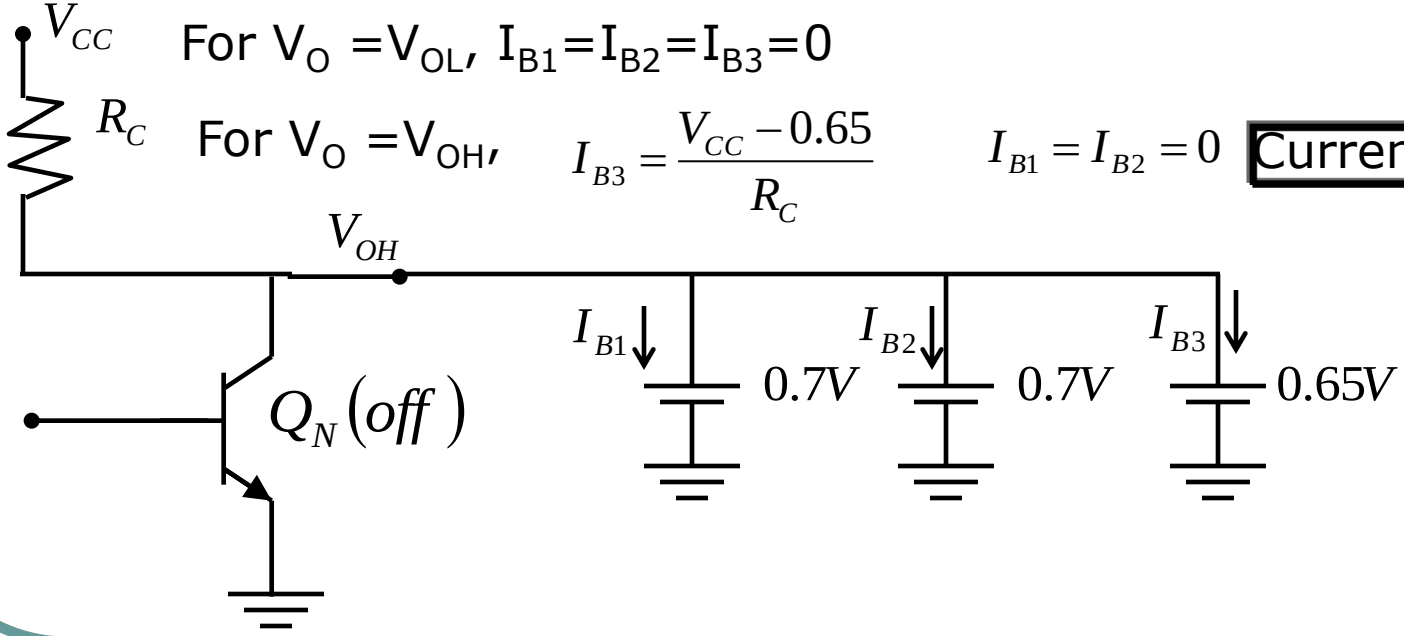
Direct Coupled Transistor Logic



- Example

Consider a DCTL RTL inverter with fan-out be three with $V_{BE1}(FA)=0.7V$, $V_{BE2}(FA)=0.7V$, $V_{BE3}(FA)=0.65V$.
Determine the base current of each load gate for output high state.

- Solution



For $V_O = V_{OL}$, $I_{B1}=I_{B2}=I_{B3}=0$

For $V_O = V_{OH}$, $I_{B3} = \dfrac{V_{CC}-0.65}{R_C}$ $I_{B1} = I_{B2} = 0$ Current hogging

- HW #5:Solve Problems: 5.8, 5.11, 5.22, 5.24, 5.27, 5.28, 5.29 (hint: neglect I_{BP})

- *Solutions of Prob. 5.24 & 5.27:*

  On the white board