Digital Electronics.

CHAPTER TWENTY FOUR

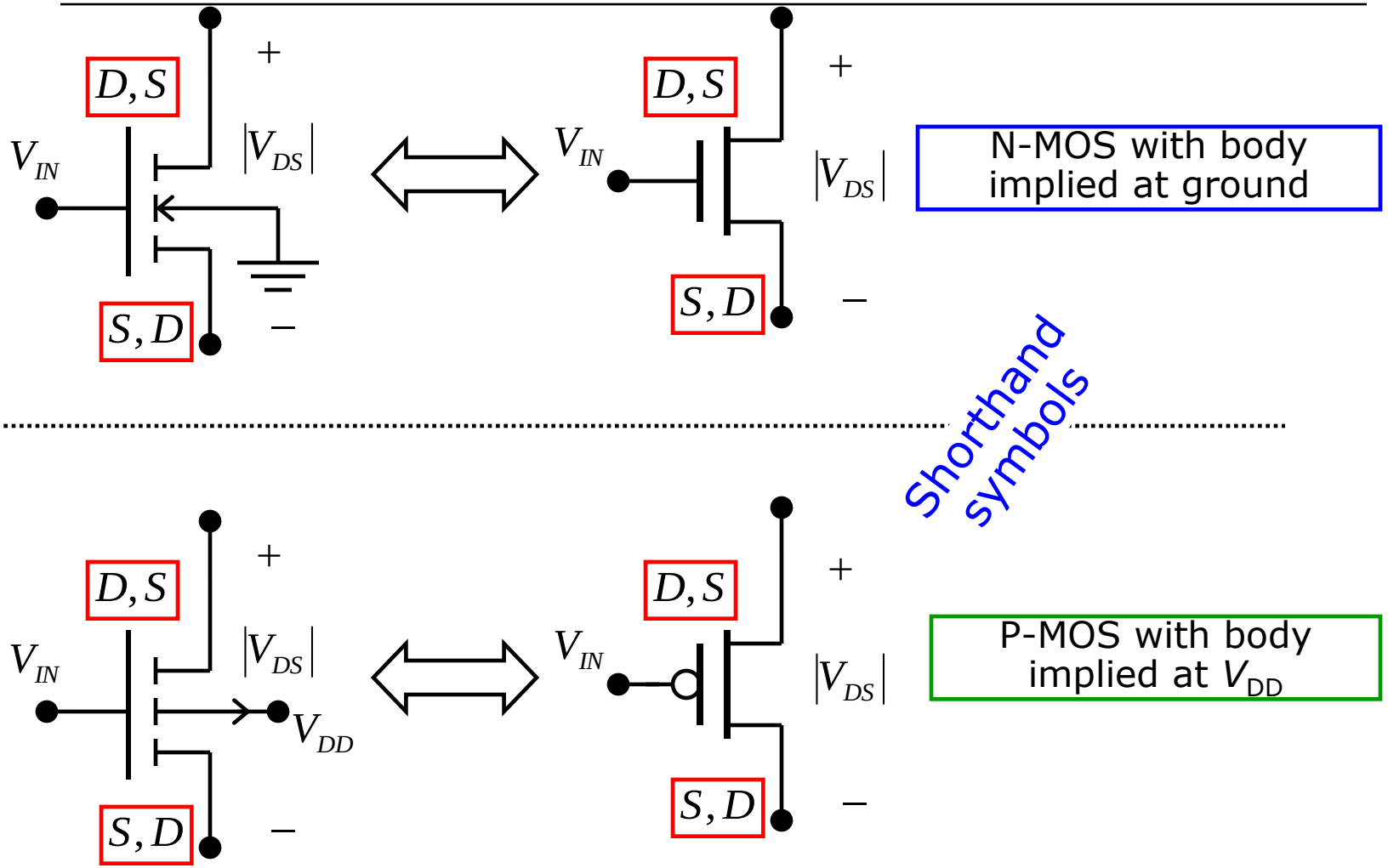
CMOS Combinational Logic Circuits

Ch. 24

Introduction

This chapter presents the structure of multi-input CMOS gates such as NANDs, NORs, AND-OR-Inverts (AOIs)

CMOS Inverter



CMOS Inverter

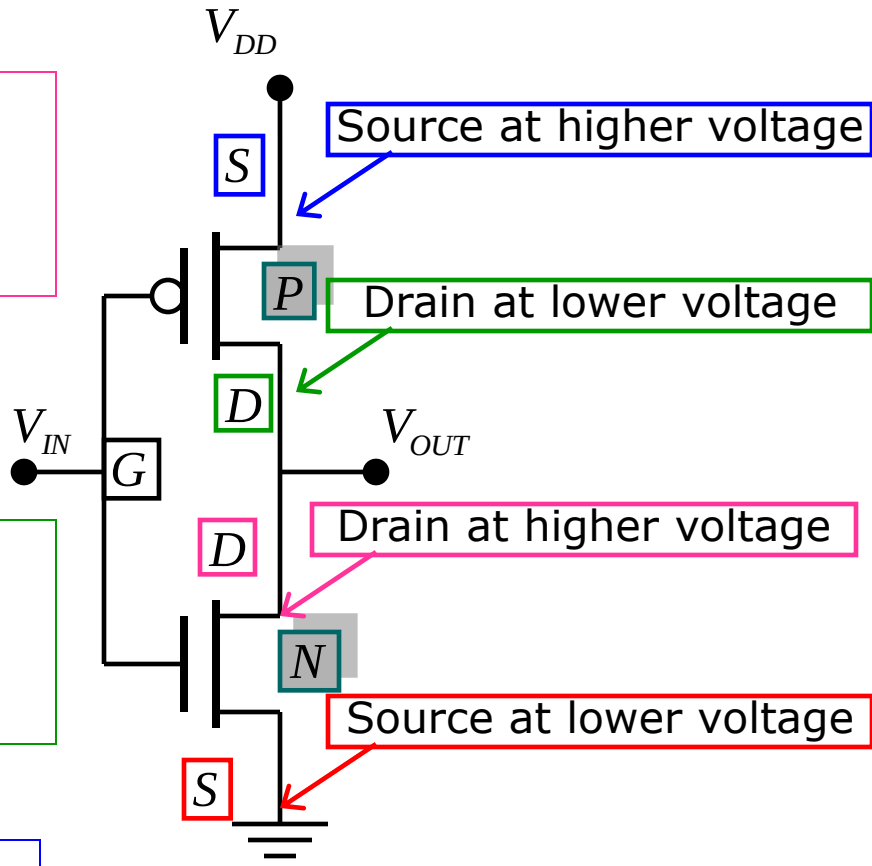
When V_{IN} is low, i.e. $V_{IN}=V_{GS}<V_{TN}$:

→ *N* is "off", *P* is active "on"

When V_{IN} is high, i.e. $V_{IN}=V_{DD}-V_{SG}>V_{TP}$:

→ *P* is "off", *N* is active "on"

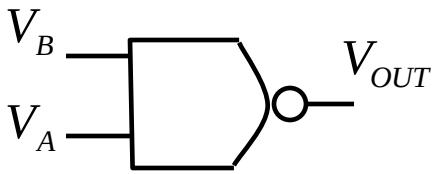
Thus, for input high and low states, both devices never conduct simultaneously

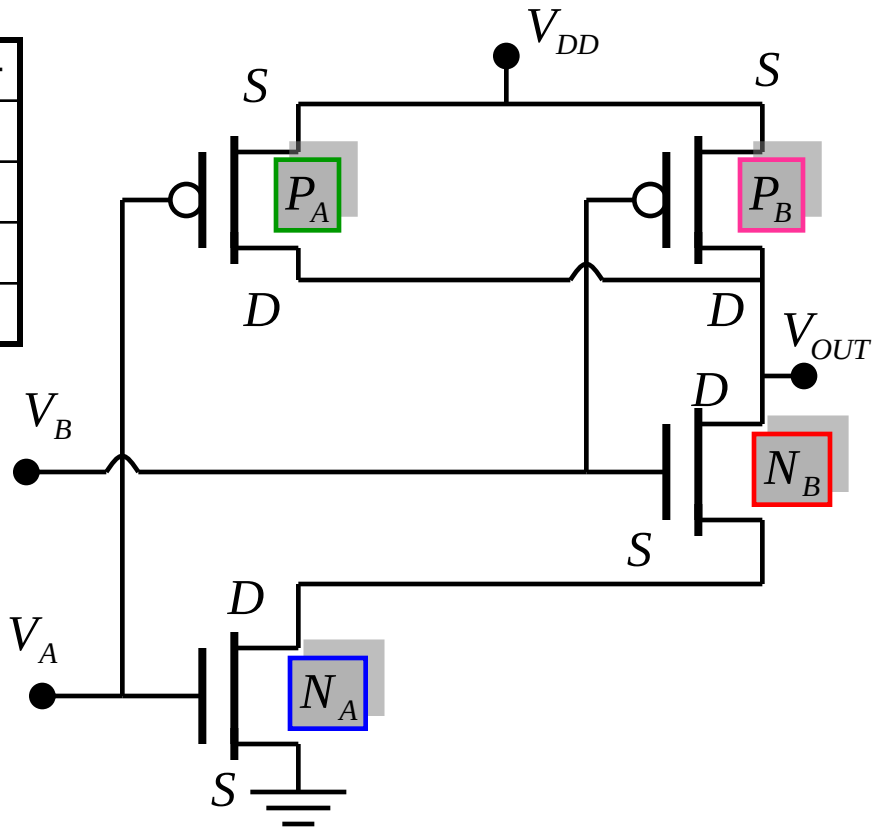


CMOS NAND Gate

V_A	V_B	N_A	N_B	P_A	P_B	V_{OUT}
low	low	off	off	on	on	high
low	high	off	on	on	off	high
high	low	on	off	off	on	high
high	high	on	on	off	off	low

NAND

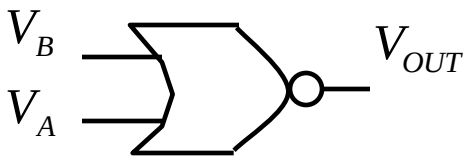


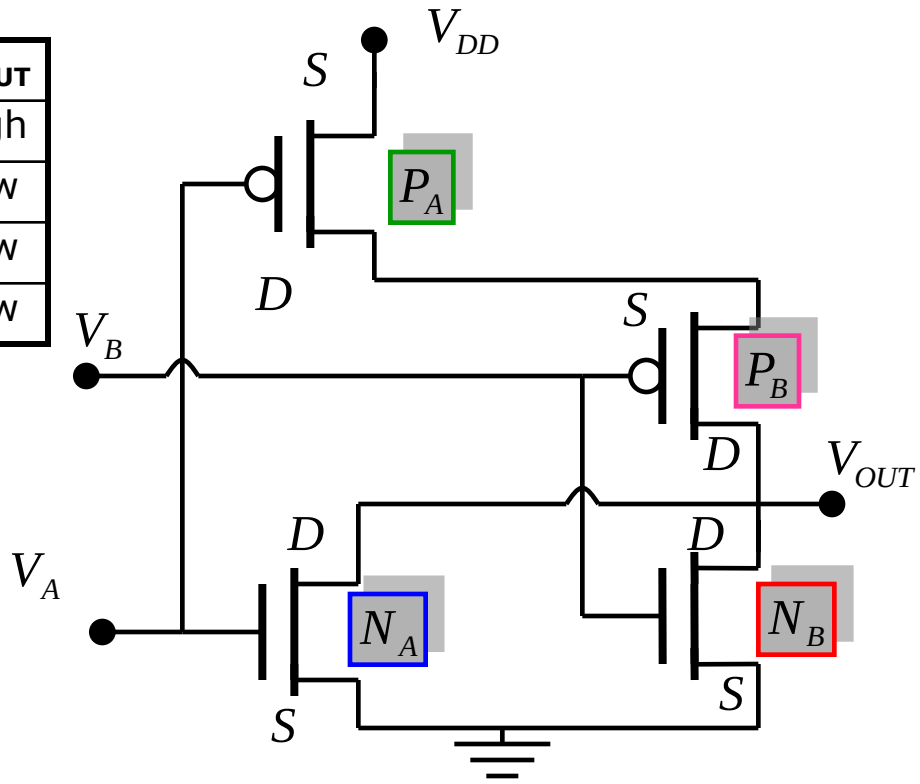


CMOS NOR Gate

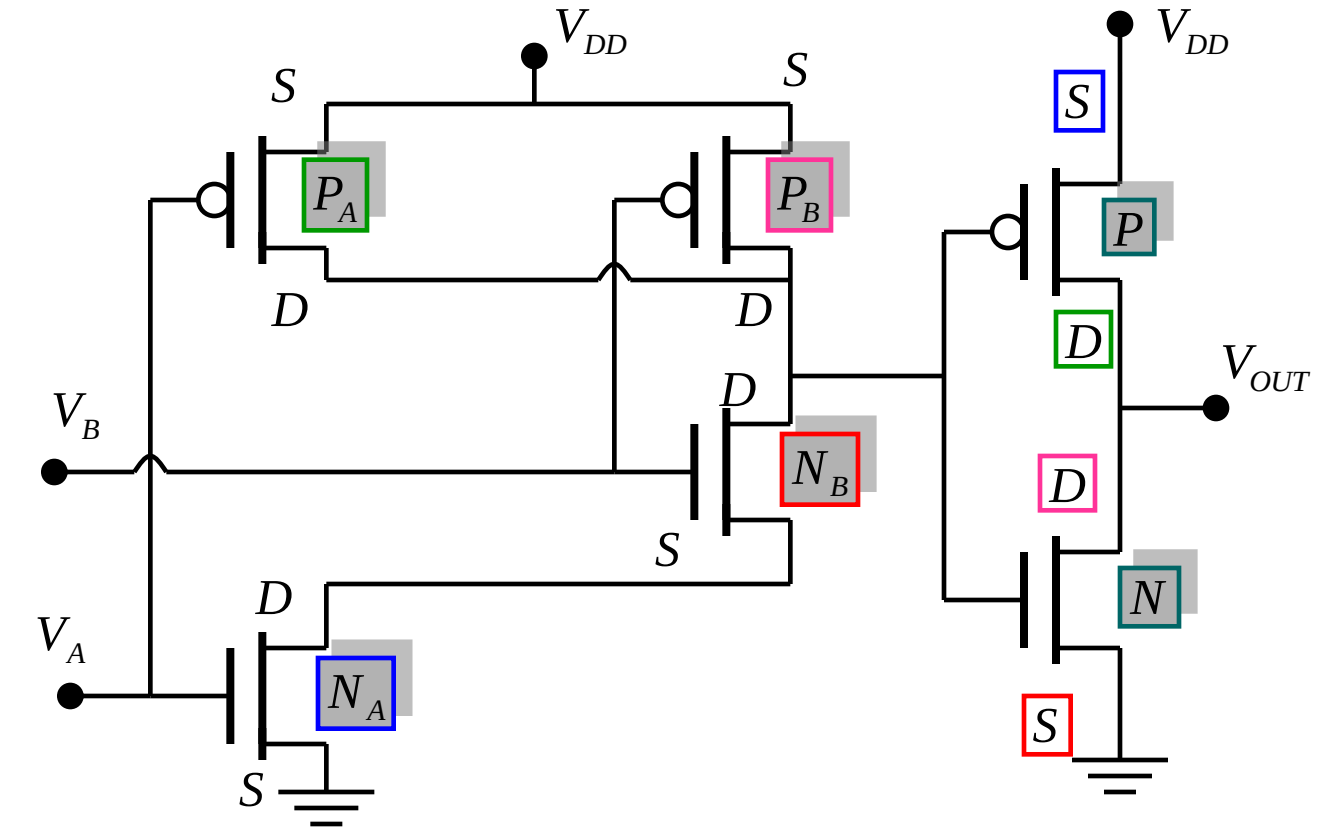
V_A	V_B	N_A	N_B	P_A	P_B	V_{OUT}
low	low	off	off	on	on	high
low	high	off	on	on	off	low
high	low	on	off	off	on	low
high	high	on	on	off	off	low

NOR

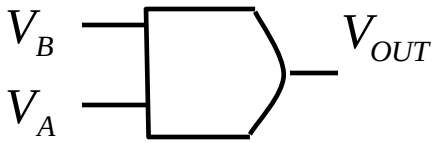




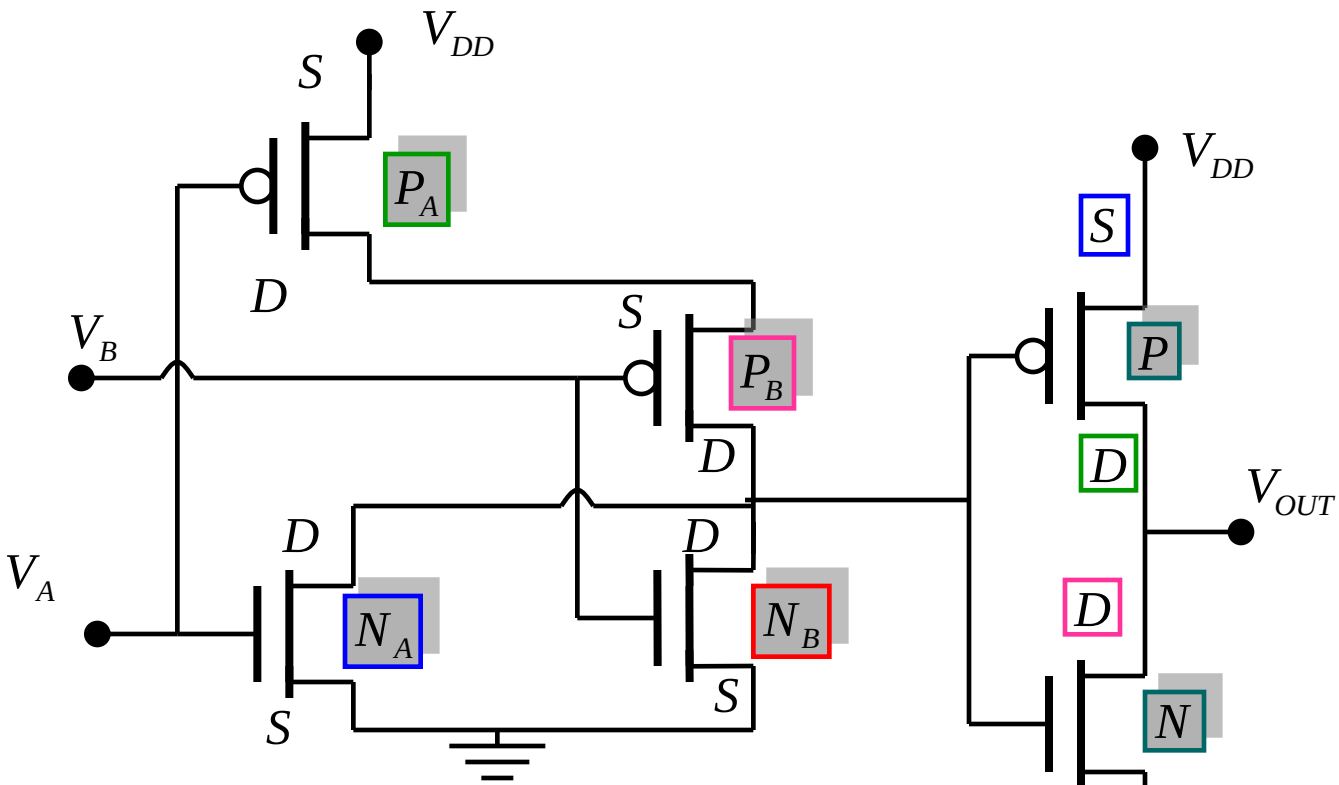
CMOS AND Gate



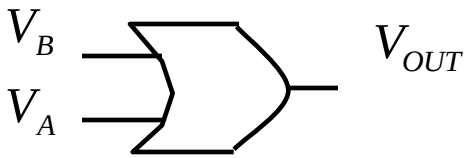
AND



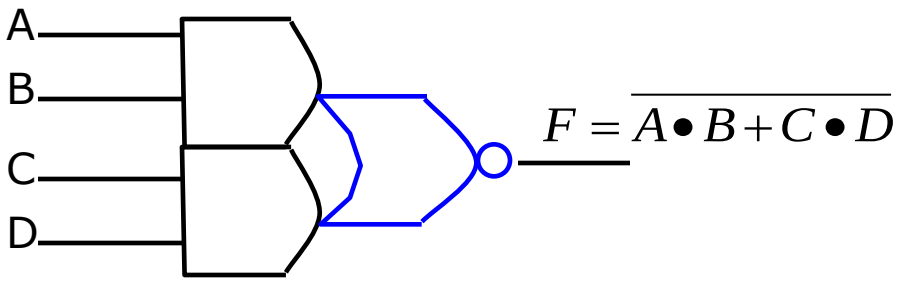
CMOS OR Gate



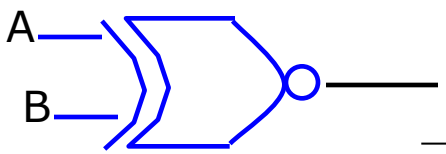
OR



CMOS AND-OR-Inverter Gate



CMOS XOR Gate



$$F = A \oplus B$$

$$F = \overline{A \bullet B + \overline{A + B}} = \left(\overline{A} + \overline{B}\right) \bullet \left(A + B\right)$$

$$F = \overline{A} \bullet A + \overline{A} \bullet B + \overline{B} \bullet A + \overline{B} \bullet B = \overline{A} \bullet B + \overline{B} \bullet A$$

- HW #13:Solve Problems: 24.**1-6**, 24.25