CHAPTER SEVENTEEN

MOS Digital Integrated Circuits

Introduction

There are several MOS logic families used in digital ICs: NMOS, PMOS, CMOS (Complementary) , HCMOS (High density and High speed).

MOSFET transistors can be used as active devices and as load elements also.

We will emphasize on N-MOSFET (enhancement) in this chapter

General N-MOS Inverter

A generalized NMOS is shown below. The load device , may be a resistor or another MOSFET.

$$V_{IN} = V_{GS} + \overset{=0}{I_G R_G} \qquad V_{IN} = V_{GS}$$

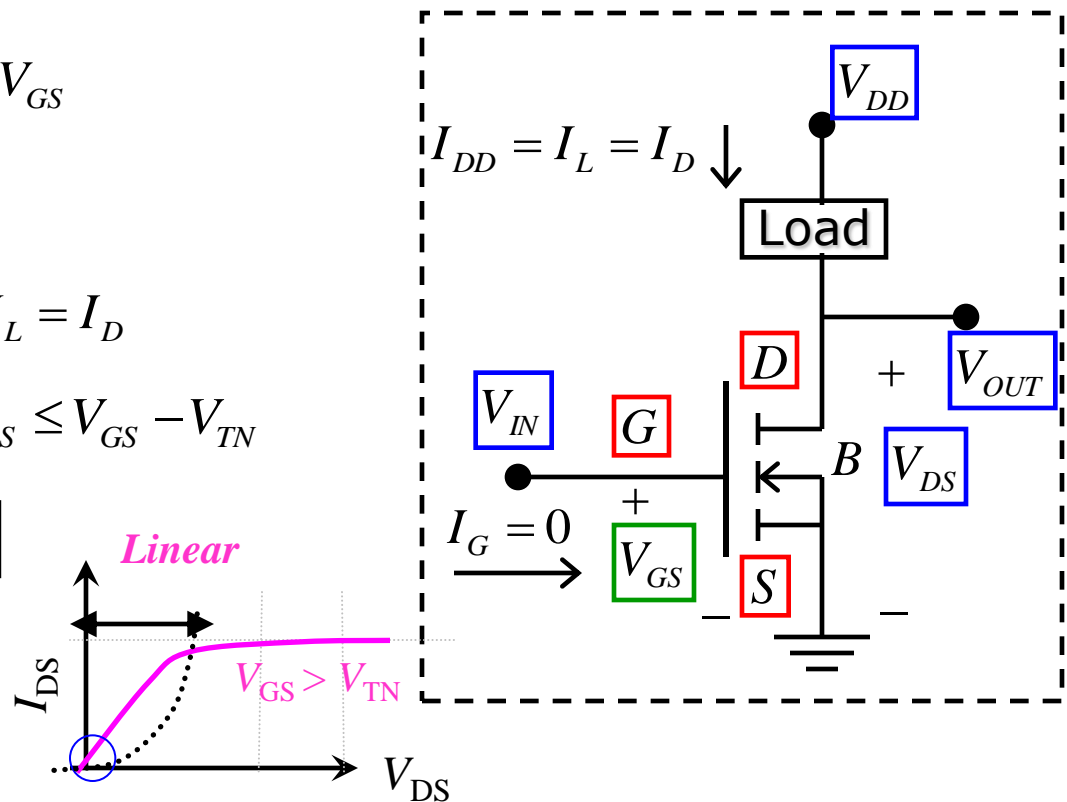$$V_{OUT} = V_{DS}$$

Since I_G is negligible $I_{DD} = I_L = I_D$

In linear mode: $(V_{GS} \geq V_{TN}), V_{DS} \leq V_{GS} - V_{TN}$

$$I_{DS} = \frac{K_n}{2}\left[2 \times (V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

Linear

In active mode: $(V_{GS} \geq V_{TN})$

$V_{DS} = 0$ Zero drain current

HOW??

I_{DS}

$V_{GS} > V_{TN}$

V_{DS}

$I_{DD} = I_L = I_D \downarrow$

V_{DD}

Load

D + V_{OUT}

V_{IN} G B V_{DS}

$I_G = 0$ + V_{GS} S

Operation of N-MOS with Zero Drain Current

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Graphical analysis:

If the drain current is forced to $I_D \sim 0$, then the drain-to-source voltage is also forced to $V_{DS} \sim 0$

Analytical analysis:

Setting $I_D \sim 0$ in the linear region gives:

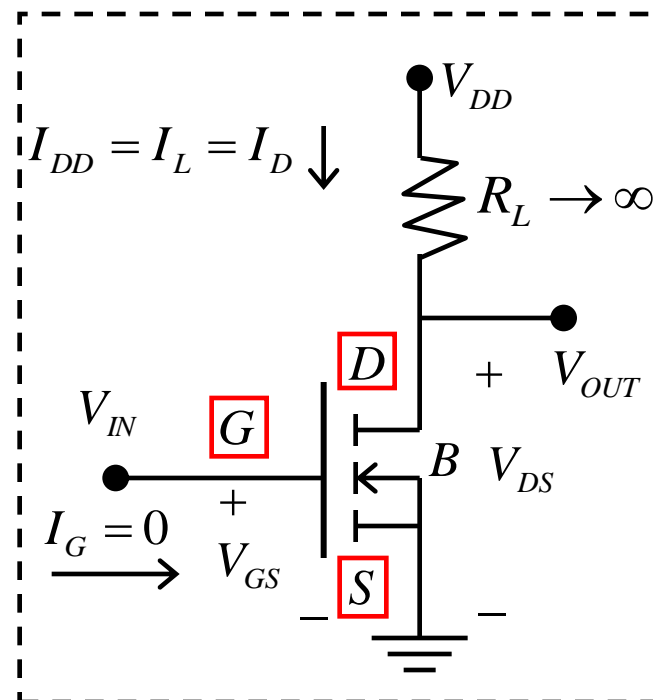$$0 = \frac{K_n}{2}\left[2 \times (V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

$$V_{DS}\left[2(V_{GS} - V_{TN}) - V_{DS}\right] = 0$$

$$\boxed{V_{DS} = 0} \quad \checkmark$$

$$V_{DS} = 2(V_{GS} - V_{TN}) \quad \times$$

Invalid since V_{DS} has to be less than $(V_{GS} - V_{TN})$

$$I_{DD} = I_L = I_D \downarrow$$

V_{DD}

$R_L \rightarrow \infty$

$+ \quad V_{OUT}$

D

V_{IN}

G

$B \quad V_{DS}$

$I_G = 0$

$+$

V_{GS}

S

Operation of N-MOS with Zero Drain Current

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Conclusion :

The use of N-MOS as an output pull-down device is important, i.e. with proper selection of a load device, high V_{GS} results in low V_{DS}.
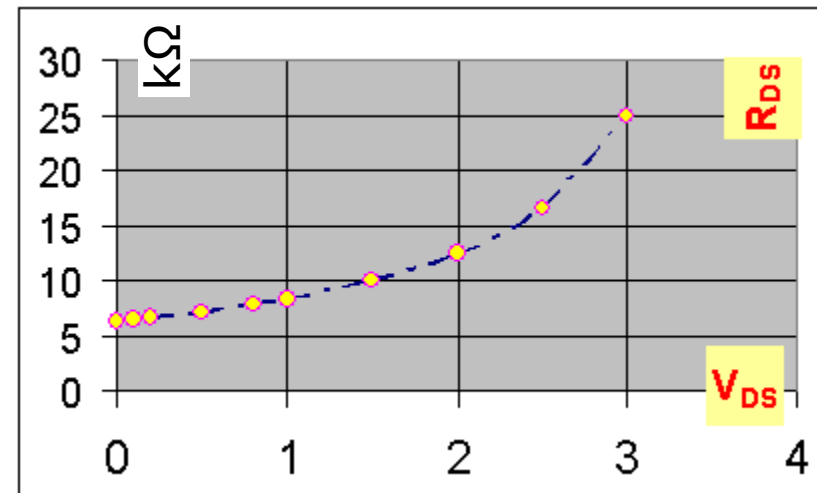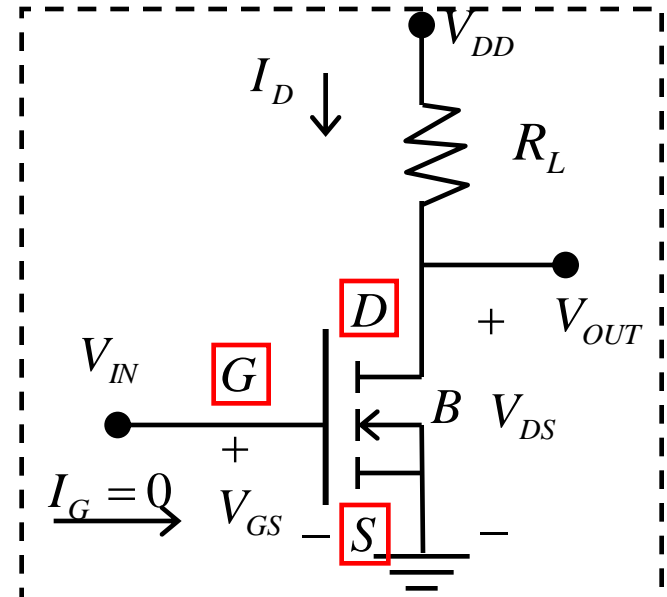
Resistance of Drain-to-Source (R$_{DS}$) Channel of NMOS Operating in Linear Mode (example):

Let : V_{GS}=5V, V_{TN}=1V, K_n=40μA/V². Determine R_{DS}

Sol:

$$R_{DS} = \frac{1}{K_n\left[(V_{GS} - V_{TN}) - V_{DS}\right]}$$

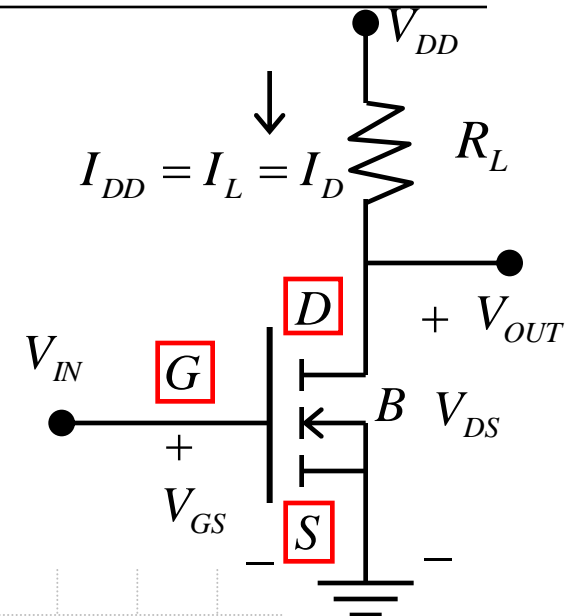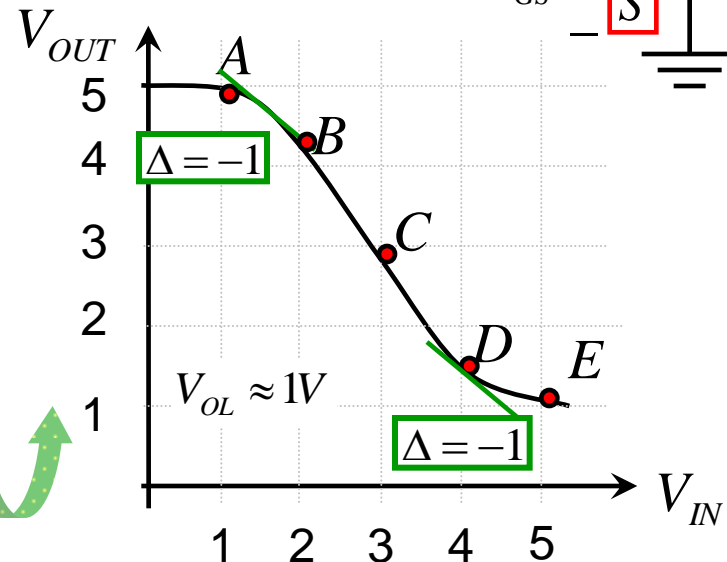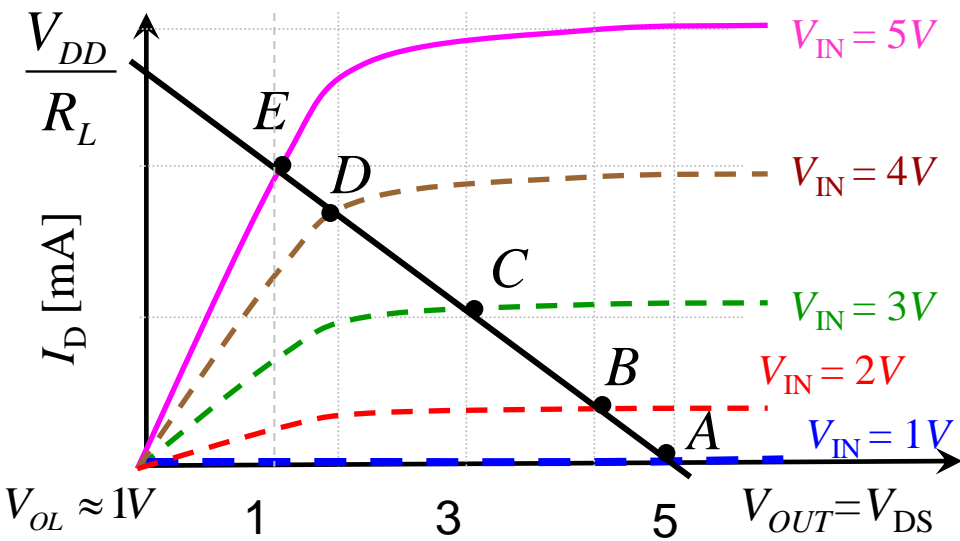It can be seen that the N-MOS operating in linear mode becomes more conductive as V_{DS} decreases.

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Graphical determination of VTC :

$$V_{IN} = V_{GS} \quad , \quad V_{OUT} = V_{DS}$$

Ch. **17**   Load line: $I_L = I_D = \dfrac{V_{DD} - V_{DS}}{R_L}$

From the intersections between the load line and the family of the current-voltage characteristics , the pairs of (V_{IN}, V_{OUT}) can be determined

$$I_{DD} = I_L = I_D$$

R_L

V_{DD}

$+ \ V_{OUT}$

D

V_{IN} G $B \ V_{DS}$

$+$

V_{GS} S

$\dfrac{V_{DD}}{R_L}$

E

D

C

B

A

I_D [mA]

$V_{IN} = 5V$

$V_{IN} = 4V$

$V_{IN} = 3V$

$V_{IN} = 2V$

$V_{IN} = 1V$

$V_{OL} \approx 1V$

1   3   5 $V_{OUT} = V_{DS}$

V_{OUT}

A

B

C

D E

$\Delta = -1$

$V_{OL} \approx 1V$

$\Delta = -1$

5   4   3   2   1

1   2   3   4   5 V_{IN}

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Analytical determination of VTC :

$\boxed{V_{OH}}$

When V_{IN} is low, i.e. $V_{IN}=V_{GS}<V_{TN}$: → N_O is cut-off

$I_L = I_D = 0$ $\boxed{V_{OH} = V_{DD}}$

$\boxed{V_{OL}}$

$I_{DD} = I_L = I_D$

R_L

$+ \ V_{OUT}$

$B \ V_{DS}$

V_{IN}

$+$

V_{GS}

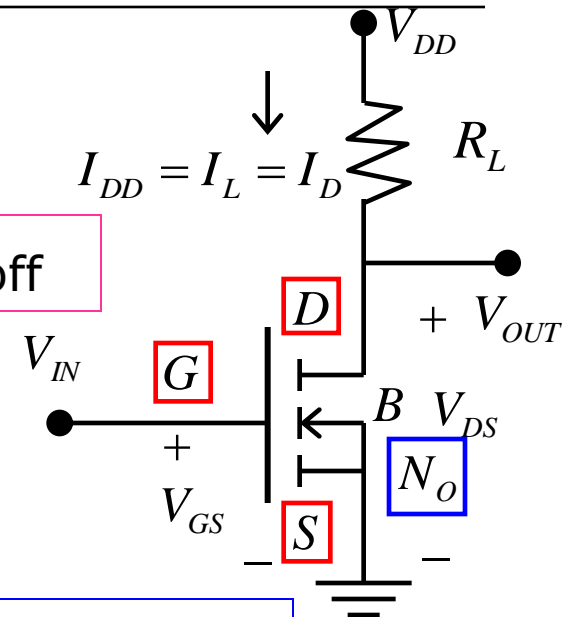$\boxed{G}$ $\boxed{D}$ $\boxed{S}$ $\boxed{N_O}$

For the low output state, the N-MOS operates in linear mode:

$$I_D = \frac{K_n}{2}\left[2\times\left(V_{GS}-V_{TN}\right)V_{DS}-V_{DS}^2\right]$$

Now, just as an assumption that the MOS is driven by a similar gate, i.e. $V_{IN}=V_{OH}=V_{DD}$.

$$I_D = \frac{K_n}{2}\left[2\times\left(V_{DD}-V_{TN}\right)V_{DS}-V_{DS}^2\right]=\frac{V_{DD}-V_{DS}}{R_L}$$

VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

$$\boxed{V_{OL}}$$

$$V_{OL}^2 - 2\left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right]V_{OL} + \frac{2}{K_n}\frac{V_{DD}}{R_L} = 0 \quad (*)$$

$$I_{DD} = I_L = I_D$$

R_L

$\boxed{D}$ $+ \ V_{OUT}$

V_{IN} $\boxed{G}$ $B \ V_{DS}$

$+$ $\boxed{N_O}$

V_{GS} $\boxed{S}$

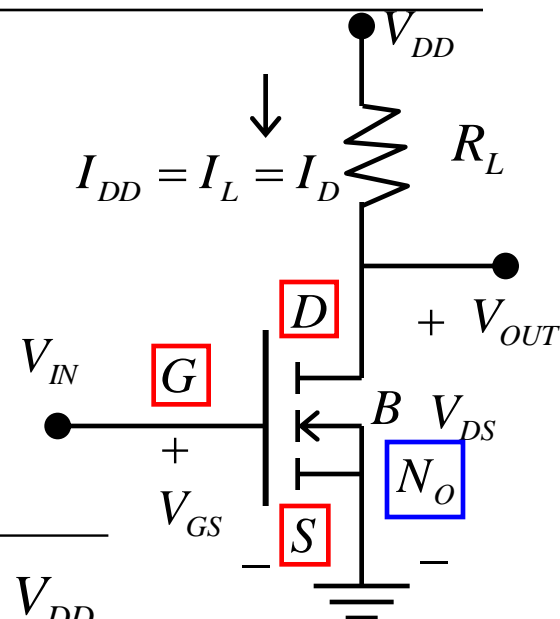$$V_{OL} = \left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right] \pm \sqrt{\left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right]^2 - \frac{2}{K_n}\frac{V_{DD}}{R_L}}$$

OR: neglecting V_{OL}^2 in (*)

$$V_{OL} = \frac{1}{K_n}\frac{V_{DD}}{R_L}\left[\frac{K_n R_L}{(V_{DD} - V_{TN})K_n R_L + 1}\right]$$

$$\boxed{V_{OL} = \frac{V_{DD}}{(V_{DD} - V_{TN})K_n R_L + 1} = V_{DS} \le (V_{GS} - V_{TN})}$$

To ensure that N_O operates in linear mode

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VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

$\boxed{V_{IL}}$

V_{IL} in MOSFET is defined as the input voltage slightly below $V_{OUT}=V_{OH}$ where slope=-1 or

$$\frac{dV_{OUT}}{dV_{IN}} = -1$$

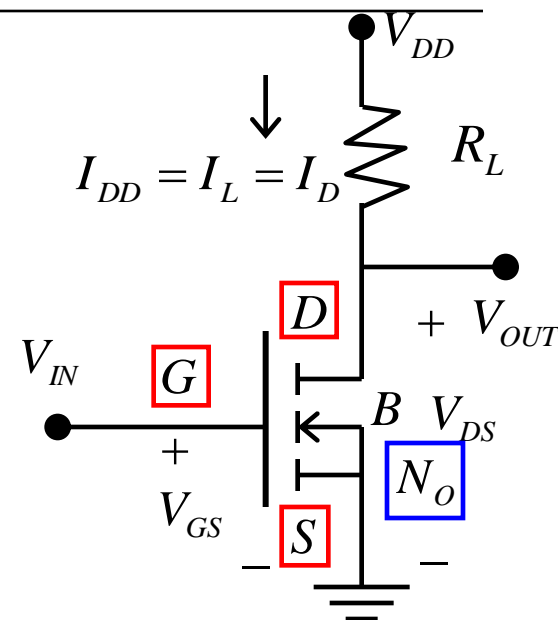For low input voltages (i.e. $V_{OUT} \rightarrow V_{OH}$), N_O is in <u>saturation</u>

$$I_D = \frac{K_n}{2}\left(V_{GS}-V_{TN}\right)^2 \Rightarrow I_D = \frac{K_n}{2}\left(V_{IN}-V_{TN}\right)^2$$

$$\&\quad I_D = \frac{V_{DD}-V_{DS}}{R_L} \Rightarrow I_D = \frac{V_{DD}-V_{OUT}}{R_L}$$

$$\frac{dV_{OUT}}{dV_{IN}} = \frac{d}{V_{IN}}\left(V_{DD}-\frac{R_L K_n}{2}\left(V_{IN}-V_{TN}\right)^2\right) = -1 \Rightarrow -R_L K_n\left(V_{IN}-V_{TN}\right) = -1$$

$$\boxed{V_{IN} = V_{IL} = \frac{1}{R_L K_n} + V_{TN}}$$

(circuit diagram)

V_{DD}

$I_{DD} = I_L = I_D$

R_L

D

$+ \ V_{OUT}$

V_{IN}

G

$B \ \ V_{DS}$

N_O

$+$

V_{GS}

S

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VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

$$\boxed{V_{IH}}$$

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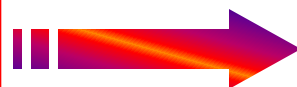V_{IH} in MOSFET is defined as the input voltage slightly before $V_{OUT}=V_{OL}$ where slope=-1 or

$$\frac{dV_{OUT}}{dV_{IN}} = -1$$

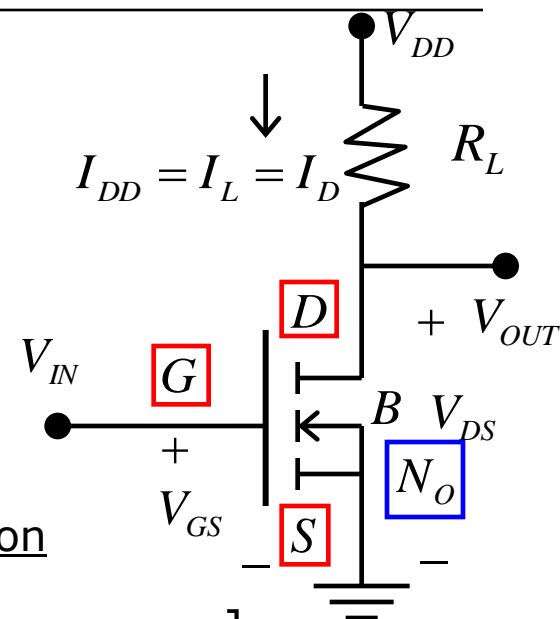For high input voltages (i.e. $V_{OUT} \to V_{OL}$), N_O is in <u>linear operation</u>

$$I_D = \frac{K_n}{2}\left[2\times(V_{GS}-V_{TN})V_{DS}-V_{DS}^2\right] \implies I_D = \frac{K_n}{2}\left[2\times(V_{IN}-V_{TN})V_{OUT}-V_{OUT}^2\right]$$

$$\& \qquad I_D = \frac{V_{DD}-V_{DS}}{R_L} \implies I_D = \frac{V_{DD}-V_{OUT}}{R_L}$$

$$\boxed{V_{OUT}(IH) = \frac{V_{IH}-V_{TN}}{2} + \frac{1}{2R_L K_n}}$$

$$\boxed{V_{IH}-V_{TN} = \frac{\dfrac{-1}{2R_L} \pm \sqrt{\left(\dfrac{1}{2R_L}\right)^2 + \dfrac{3}{2}\dfrac{V_{DD}}{R_L}K_n}}{\dfrac{3}{4}K_n}}$$

$$\text{must } V_{DS} \le (V_{GS}-V_{TN}) \qquad \boxed{\text{i.e. } V_{OUT}(IH) \le (V_{IH}-V_{TN})}$$

Circuit labels: V_{DD}, $I_{DD}=I_L=I_D$, R_L, D, $+ \; V_{OUT}$, V_{IN}, G, B, V_{DS}, N_O, $+$, V_{GS}, S

VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

$\boxed{V_M}$ Mid point

$$V_{OUT} = V_{IN} = V_M$$

$\Longrightarrow$ $V_{DS} = V_{OUT} = V_M$ & $V_{GS} = V_{IN} = V_M$
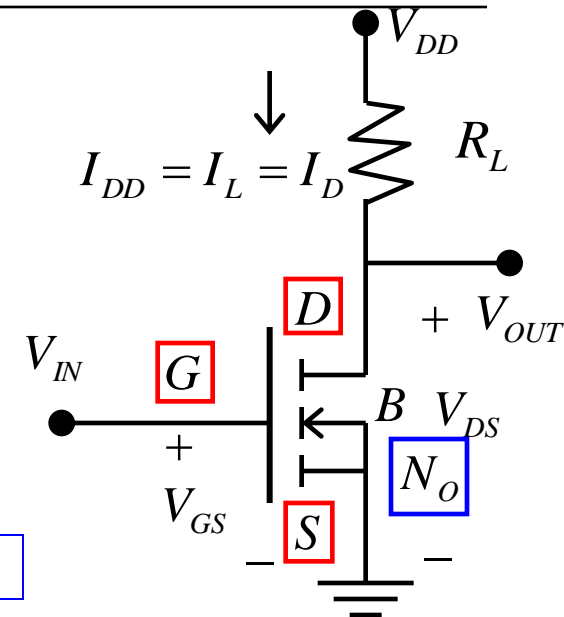
$$V_{DS}(sat) = V_{GS} - V_{TN}$$
$$= V_{DS} - V_{TN}$$

$\blacktriangleright\!\!\!\blacktriangleright$ $V_{DS}(sat) < V_{DS}$ $\boxed{\text{N}_O \text{ is in } \underline{\text{saturation operation}}}$
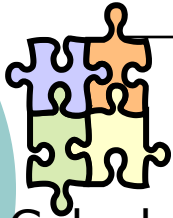
$$I_D = \frac{K_n}{2}\left(V_M - V_{TN}\right)^2 \quad \& \quad I_D = \frac{V_{DD} - V_M}{R_L}$$

$$\frac{K_n}{2}\left(V_M^2 - 2V_M V_{TN} + V_{TN}^2\right) = \frac{V_{DD}}{R_L} - \frac{V_M}{R_L}$$

Then solve for V_M

V_{DD}

$I_{DD} = I_L = I_D$ R_L

$\boxed{D}$ $+$ V_{OUT}

V_{IN} $\boxed{G}$

B V_{DS}

$+$ $\boxed{N_O}$

V_{GS} $\boxed{S}$

$-$ $-$

VTC of N-MOS Loaded with Resistor

○ Example

Calculate the critical values of the VTC of a resistor loaded NMOS inverter shown previously assuming:

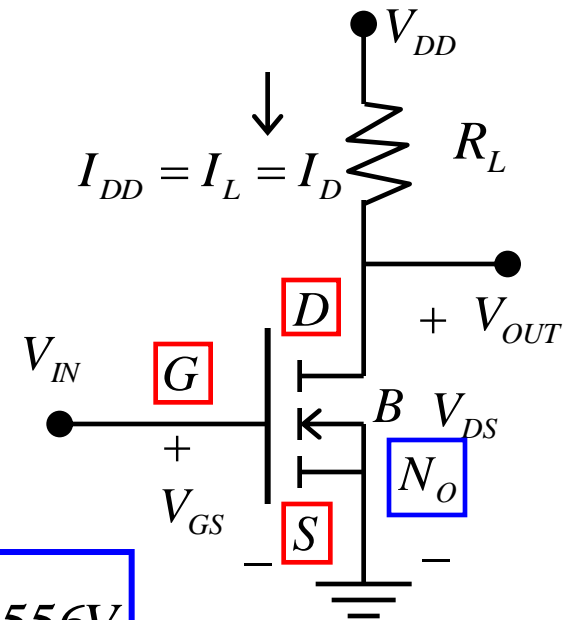V_{DD}=5V, V_T=1 V, k_n=40μA/V² , R_L=50kΩ,

○ Solution

$$V_{OH} = V_{DD} = 5V$$

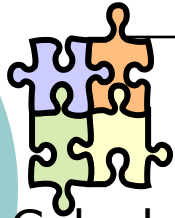$$V_{OL} = \frac{V_{DD}}{(V_{DD} - V_{TN})K_n R_L + 1} = \frac{5}{(5-1)40 \times 10^{-3} \times 50 + 1} = 0.5556V$$

$$V_{IL} = \frac{1}{R_L K_n} + V_{TN} = \frac{1}{50 \times 40 \times 10^{-3}} + 1 = 1.5V$$

$$I_{DD} = I_L = I_D$$

V_{DD}

R_L

D

$+\ V_{OUT}$

V_{IN}

G

$B\ V_{DS}$

$+$

N_o

V_{GS}

S

$0556 \le (5-1) ok!$

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VTC of N-MOS Loaded with Resistor

○ Example

Calculate the critical values of the VTC of a resistor loaded NMOS inverter shown previously assuming:

V_{DD}=5V, V_T=1 V, k_n=40μA/V² , R_L=50kΩ,

○ Solution

$$V_{IH} - V_{TN} = \dfrac{\dfrac{-1}{2R_L} \pm \sqrt{\left(\dfrac{1}{2R_L}\right)^2 + \dfrac{3}{2}\dfrac{V_{DD}}{R_L}K_n}}{\dfrac{3}{4}K_n}$$
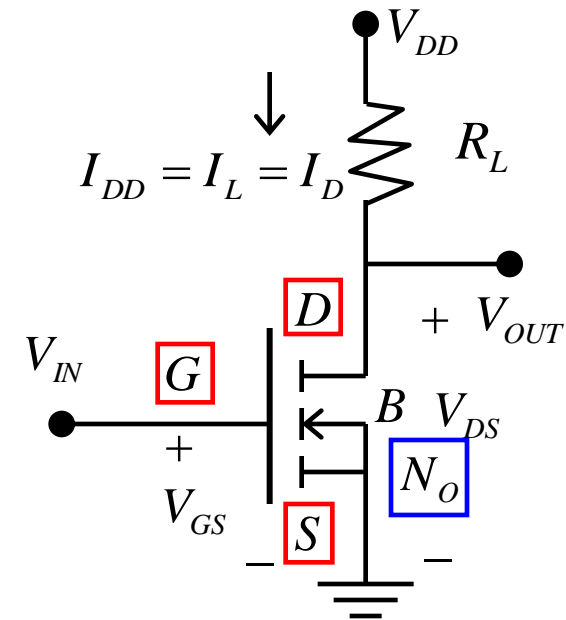
$$V_{IH} - V_{TN} = 2.27 \quad \text{or} \quad -2.94$$
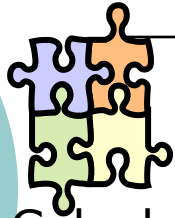
$$V_{IH} = 3.27 \text{ V}$$

$$V_{OUT}(IH) = \frac{V_{IH} - V_{TN}}{2} + \frac{1}{2R_L K_n} = \frac{2.27}{2} + \frac{1}{4} = 1.39V$$

$$\text{must } V_{DS} \leq (V_{GS} - V_{TN}) \quad ok!$$

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$I_{DD} = I_L = I_D$

R_L

V_{DD}

D

$+ \quad V_{OUT}$

V_{IN}

G

$B \quad V_{DS}$

N_O

$+$

V_{GS}

S

$-$

$-$

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VTC of N-MOS Loaded with Resistor

○ Example

Calculate the critical values of the VTC of a resistor loaded NMOS inverter shown, assuming:

V_{DD}=5V, V_T=1 V, k_n=40μA/V^2 , R_L=50kΩ,

○ Solution

Solve for V_M

$$\frac{K_n}{2}\left(V_M^2 - 2V_M V_{TN} + V_{TN}^2\right) = \frac{V_{DD}}{R_L} - \frac{V_M}{R_L}$$

$$V_M = 2.56V$$

$$I_{DD} = I_L = I_D$$

V_{DD}

R_L

D

$+ \ V_{OUT}$

V_{IN}

G

$B \ V_{DS}$

$+$

V_{GS}

S

N_O

$-$

$-$